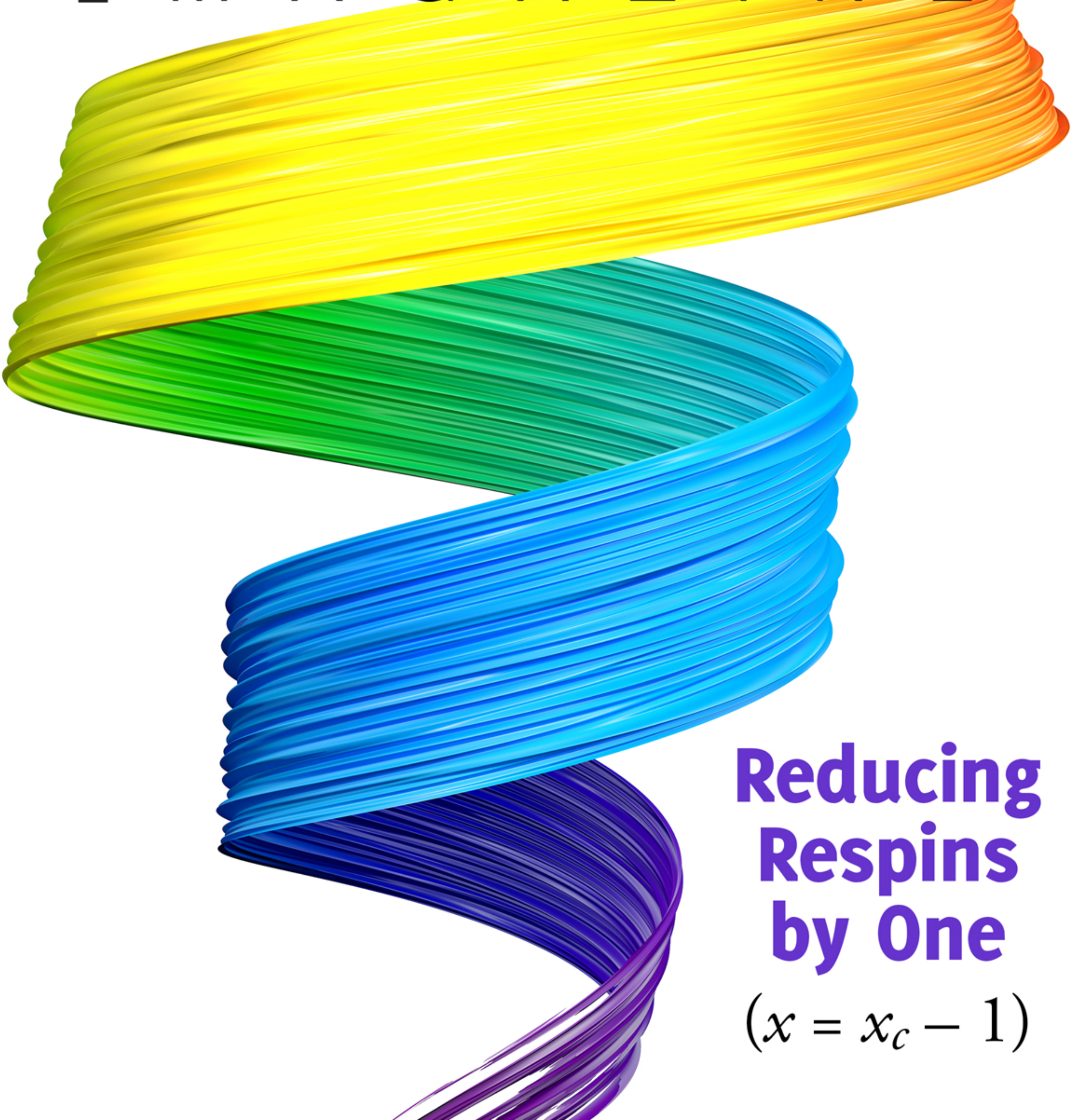
DECEMBER 2020

I-Connect007

DESIGN007 MAGAZINE



Reducing Respins by One

$(x = x_c - 1)$

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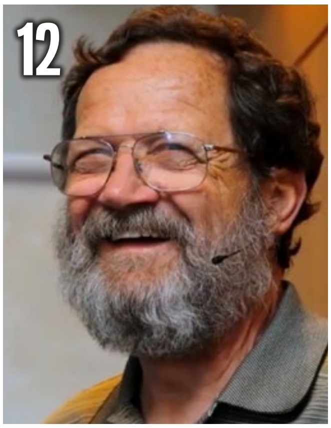
[1] IPC. (2017). Findings on the Skills Gap in U.S. Electronics Manufacturing.

DESIGN007 MAGAZINE

Reducing Respins by One

Designers have been talking about eliminating PCB design respins for decades. Cutting respins was just one of the many benefits that were slated to accrue when PCB designers began adopting solid DFM practices in the 1990s. But today, OEMs routinely go through two, three, or more PCB design respins. This month, we delve into the idea of reducing respins by one: $x = x_c - 1$.



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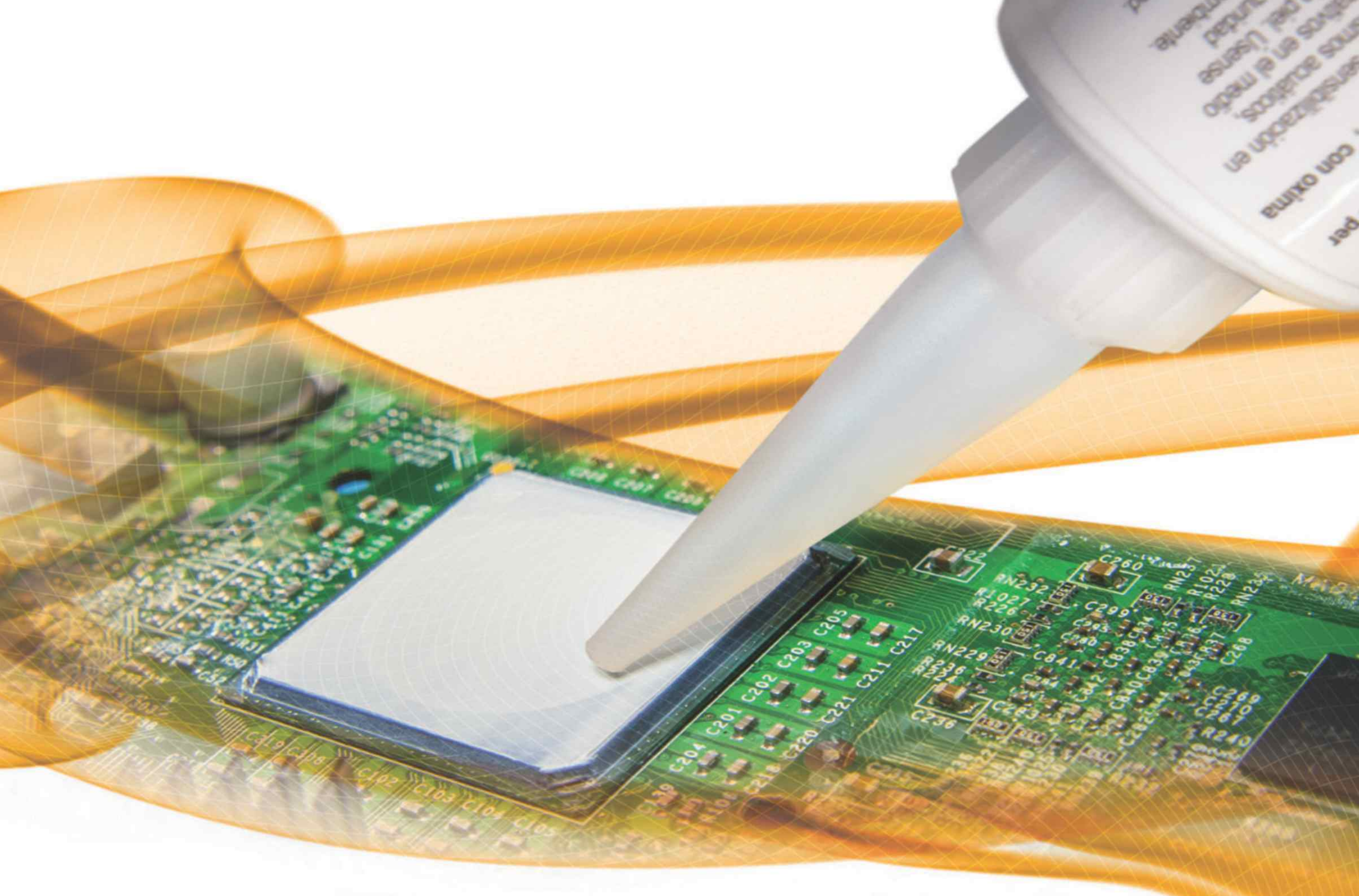
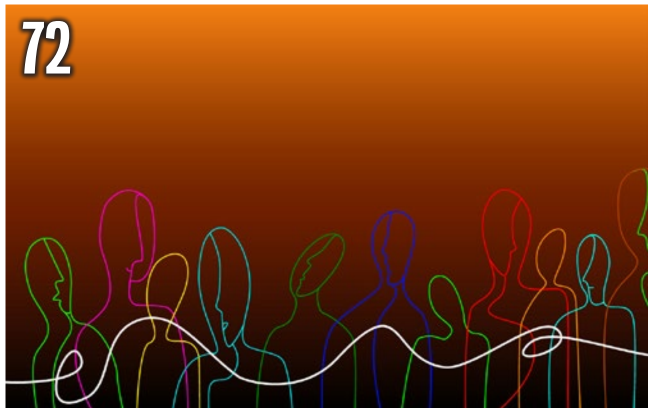
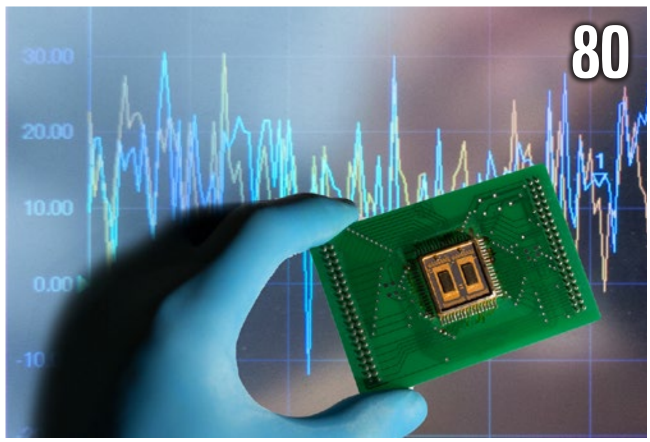


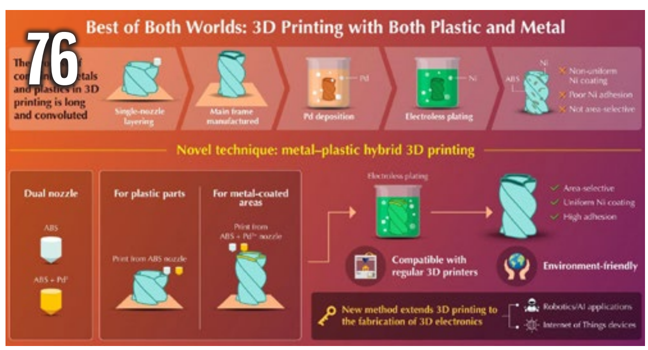
FLEX007

This Month in Flex

Flexible and rigid-flex circuits are a double-edged sword. They offer a multitude of dynamic options that rigid boards can't match—and far more ways to wind up with costly, unnecessary respins. With flexible circuits, solid DFM techniques are more critical than ever.







What If We Reduced Respins by One Globally?

The Shaughnessy Report

by Andy Shaughnessy, I-CONNECT007

This is hardly a new topic. We've been talking about eliminating PCB design respins for decades.

When I first started covering this industry over 20 years ago, DFM was all the rage. Cutting respins was just one of the many benefits that were slated to accrue when PCB designers adopted solid DFM practices.

Designers were no longer going to throw designs "over the wall." Designers would talk to CAM departments throughout each design, design data would arrive at CAM optimized for that fabricator's processes, and songbirds would sing in perfect harmony.

Lee Ritchey and John Zazio even penned a textbook, *Right the First Time: A Practical Handbook on High-Speed PCB and System Design,* full of tips and techniques for eliminating respins. We could almost see the finish line. It sounded too good to be true…and it was.

After 20 years of constantly talking about DFM, the disconnect between designer and fabricator is wider than ever. Some OEMs routinely go through two, three, or more PCB designs. Just try to find a CAM engineer who doesn't have a dozen recent horror stories regarding bad designs and design data. Lee and John could probably edit them into a much larger book called *Wrong the First, Second, and Third Times.*

A September 2018 article in *Lifecycle Insights* put the average number of PCB design respins at 2.9. If this figure is accurate, I imagine that a few companies have eliminated respins completely, but some OEMs are experiencing five or six spins per design.

But we really can't blame designers for a situation that they didn't create. Many times, the designer's company has budgeted for two or three respins. The design gets out the door faster, and the designer can go to work on the next project. So, why focus on reducing respins by one?

It all started during a meeting to plan an issue on new DFM techniques. "What if every OEM in the world reduced their respins by just one? What would that save, not just in wasted revenue, but in other resources like hours or time to market?"

After a long pause, we did some back-of-the-napkin calculations and realized that we'd need a bigger napkin. It's impossible to gauge the savings from cutting one respin worldwide, but it would have to be a huge

number. I imagine we'd be talking about hundreds of millions of dollars in savings worldwide—just from reducing respins by one. When you account for the savings in wasted hours and gains in time to market, you start to get an idea of the cost of multiple respins, even if your company can "afford" the lost revenue.

The idea of reducing spins by one is applicable across the entire industry, including reducing process steps, scrap, and failure rates in fabrication and assembly. We discovered that this concept has a mathematical name (if you can call it that): $x = x_c - 1$. It's not the catchiest catchphrase, but it describes what we're talking about perfectly, and we'll continue to explore this theme throughout 2021.

If you design boards for an OEM that routinely experiences two or three respins, consider starting your own $x = x_c - 1$ plan. It's not complicated: Just work on cutting your respins by one, and then look at the data. What did you learn? What worked, and what didn't work? Why couldn't you cut one more respin?

This month, we delve into the idea of reducing respins through solid DFM techniques. We start with our interview with Lee Ritchey, who discusses the hidden costs of extra respins, how to avoid them, and whether an MBA or an engineer is the best person to lead a technology company. Next, Chris Young of Young Engineering Services offers some techniques for avoiding respins and explains why, with multiple respins, lost revenue is just the tip of the iceberg.

Then, we have a conversation with Michael Ford and Happy Holden, who discuss the new DPMX standard, and how the digital twin can help designers work more efficiently. And Tara Dunn focuses on the need to communicate "outside the box" for proper flexible circuit DFM.

The idea of reducing spins by one could be the start of a movement. If you've managed to cut one respin from your design cycle, I'd like to hear how you did it.

It's been a hell of a year. If we can all cut process steps by one, we can make 2021 a fantastic year. Have a great holiday! **DESIGN007**

Andy Shaughnessy is managing editor of *Design007 Magazine.* He has been covering PCB design for 20 years. He can be reached by clicking here.

Lee Ritchey on Reducing Respins by One

Feature Interview by the I-Connect007 Editorial Team

I-Connect007 recently spoke with Lee Ritchey about the subject of continuous improvement with a focus on DFM, specifically looking at the benefits of reducing the number of respins by just one. A longtime instructor and one of the authors of *Right the First Time: A Practical Handbook on High-Speed PCB and System Design*, Lee has spent decades preaching the value of solid DFM practices, so we asked him to discuss why so many OEMs accept multiple respins with each design project and what designers could do to eliminate just one spin. He also shares some of the lessons in reducing respins that he learned in the early days of Silicon Valley.

Andy Shaughnessy: We've been talking about making 2021 the year of continuous improvement, and we came up with an idea. What if we eliminated just one spin from every cycle and kept that as a goal? Of course, your book Right the First Time came to the top of our conversation. Many companies continue to build respins into the project budget, but what about the wasted hours?

Lee Ritchey: You picked a topic that I actually know something about. I have stories. Some of them are horror stories! But if you have one less respin than the competition, you're at the market first. That has been historically the business model of Intel and IBM. Of course, Intel and AMD have roughly the same kind of processors, with one exception: AMD has never been first to market.

Originally, that was because they had to spin the silicon a couple of times. The people at Intel realized the person who's first to market gets to define the playing field, and they spent huge amounts of money on simulation tools.

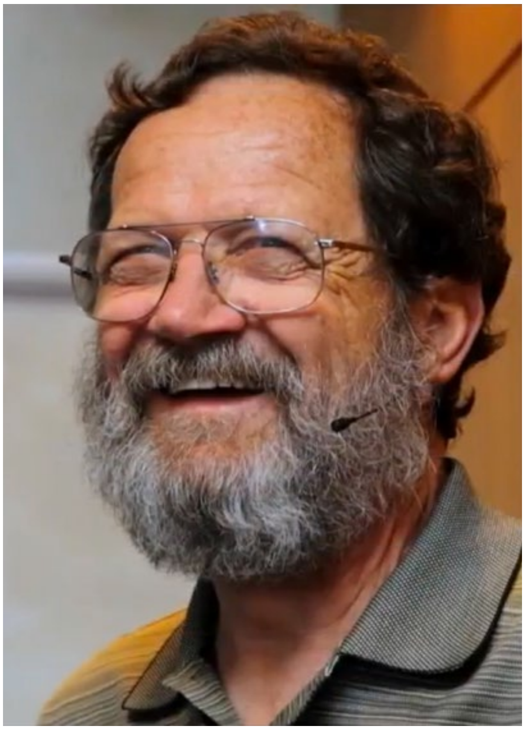
One of my favorite stories is the first Pentium processor. It was the first time a processor had been shipped on the first artwork. They got a lot of press on that. During the press conference, somebody asked how they did it, and the project manager said, "We didn't cut silicon until we got a DOS prompt on the emulator." They spent the money on upfront design, and that's sort of defined that field ever since.

There were two where I have really clear experience. One of them was with 3Com, where they would assume they were going to spin the design and rush to get a prototype. The usual reason was so that the engineers

had something to work on, and almost never was that something right.

I did a brief piece on this, which wasn't even a respin; it had to do with how much money we spent to accelerate getting the prototype of a PCB. In the case I was working on there, the difference between a three-day turn and a 10-day turn was only about $5,000, and they wouldn't spend it.

One evening, we were doing the budget for the next quarter, and it came out to a little bit less than $2 million a week to run the project. I told management, "If I spend $5,000 and take a week out of this budget, doesn't that make good sense for our return on investment?" Finally, someone had quantified the cost of time for them because no one had done that.


Lee Ritchey

When I took over engineering at Maxtor, they had built into their budget six spins of the prototype. I asked them why they had done six spins. They would hand over a schematic to the layout people, and all the resistors were TBD. "When are you going to find out?" "After we get the board, we'll figure that out." That was a massive operation. That was how they operated. They were up against Western Digital and Seagate, and both of those companies were doing analytical work, and the rest is history. There is no Maxtor.

And that's not even a respin; that's just being smart about where you spend premiums. Now, that gives you a yardstick for how much a respin costs. If you're lucky, and a respin only takes six weeks and $2 million, isn't it worth spending another week getting it right? I think so.

Barry Matties: What does it take to get it right to begin with? What's the recipe?

Ritchey: Analysis. In the case of the microprocessor, they built an emulator and ran the software on the emulator to make sure that the two worked together correctly before cutting the two of them. In the case of the box at 3Com, it was a question of taking long enough to make sure you had all the design rules right and that the netlist is correct. Another example, which is more painful because it made a company disappear, was at Maxtor. At the time, there were eight companies in the disk drive business, all trying to make the same thing.

Matties: Why would a company allow so many respins? Is doing it right the first time that challenging?

Ritchey: No, but their managers are not engineers.

Matties: But even aside from engineers, if you just take the economics, you don't have to be an engineer to do the math.

Ritchey: If you look at those companies, they are run by people with MBAs and degrees in finance, not engineering. That's what undoes them.

Matties: They should be able to look at it and see that a respin is going to cost them millions of dollars. It seems that their math sensibilities would kick in.

Ritchey: You would think so, but that's not how it works. Bob Noyce said this more than once when Silicon Valley was having a lot of failures. There was a forum we used to have once a month in the evening to discuss problems with businesses in the valley.

Bob said, "The worst thing that happened to Silicon Valley was the Harvard MBA." We said, "What do you mean?" He explained, "They teach these people that if you have an MBA, you can manage anything."

Of course, that's not true. If you don't understand the technology, you're not going to make the right choices. The people who are put in charge of these companies have MBAs, and they don't know anything about technology; they just write schedules, and you have to live with them, whether they're realistic or not.

Then, it doesn't work on the first spin. There's all this agony in, so they do it again. No one learns from that. If you look at those companies, they just keep doing it that way until a competitor eliminates them.

Matties: What do you think is the average number of respins? I know it's a broad question, but if you look at the industry, what's the typical respin in the industry?

Ritchey: I can only speak about the companies my partner John Zazio and I work with, and that's zero. We have failed if we have to respin a board. But I will tell you about a company that I have been working with. I can't say the company's name, but they spin the board 14 times.

Matties: How are they still in business?

Ritchey: I asked the same question. About half of them weren't working, and one person who wasn't working was the chassis designer. It didn't fit in the box. But I almost fell out of my chair when I heard the answer: They don't have a competitor. They wouldn't be here if they had a competitor.

Matties: They're allowed to not learn from their mistakes.

Ritchey: When I was at Maxtor, I tried to explain to them that if we take a little longer and get this thing right, we can get ahead of the competition. I told them, "The first competitor who does that will wind up defining the field," and sure enough, it happened.

Matties: In your classes, do you ever ask the attendees how many respins they do?

Ritchey: I never thought to ask that question, but I can give you some yardsticks. The first step you have to take for respin is you must fix the artwork. Then, you have to go through a fab cycle and then an assembly cycle. It is rare that you get a turnaround of a week at a fab shop, and the same is true for assembly.

Of course, how long a CAD department takes depends on how big the error is. If you're lucky, it will be three weeks. Now, you have to multiply that by the cost of all the people on the project because they're all sitting on their hands until that prototype shows up, including sales.

Matties: That's the lost opportunity.

Ritchey: They're sitting on their hands waiting for this thing, and that's money the company is going to spend.

Dan Feinberg: What do you think the average number of respins is?

Ritchey: I don't know how to answer that. But as soon as you can accurately describe what the real cost is, then people can put their number of respins in context.

Feinberg: That's the break-even time metric; the MBAs understood that.

Happy Holden: Hewlett and Packard both understood engineering, but they also understood first to market and profitability and total system costs, not just how much you spend on wages.

Ritchey: HP was really good at this for a very long time. I have a scholarship program in our university called a Hornet Leadership Program. The reason is that I've seen dozens of companies crash because the engineers who conceived the ideas that made the company wouldn't lead the company. They would make somebody else come in and lead, and that would be the Harvard MBA or somebody like that who did not understand what was going on.

HP is a good example, and so is Intel. The engineers who started did not give up the leadership role. They surrounded themselves with the skills they did not have. That's what a good tech company looks like. The ones that are failing are the ones where the engineers didn't lead. The manufacturing people who were louder than all the rest wound up in front of the company, and they bankrupted it. Engineers must lead and quantify what things cost because nobody else has this information.

I sometimes say this in my class: "No one in their right mind would ever think of putting an engineer in charge of a bank." Why do you put a finance person in charge of an engineering company? I can cite a dozen companies that have failed because of that.

Engineers must lead and quantify what things cost because nobody else has this information.

Matties: You've mentioned several points about the economics of a respin. But what are some other benefits from eliminating respins beyond the money side of it?

Ritchey: If you eliminate the respin, then your next product can be on the market sooner because those people can start on the next products sooner, which is what we did at disk drives. Back when I was part of it, the production life of a disk drive was nine months, so we had to have the next one ready in nine months. If your team was tied up for three or four months on a respin, you had a three-month gap and no new product.

Matties: Is there something, though, that the engineers and designers can do to get it right the first time? And even though companies are budgeting for respins, what can the engineer do to avoid it, or is he just bound by broken systems?

Ritchey: Engineers must have enough skill, first of all. For example, in a disk drive, you have servos, and you must have somebody who understands how to design a stable servo loop and that kind of thing, and that's one of the things they weren't doing. It requires enough skill to avoid trial and error. In almost all cases, the skill set is what's missing.

Matties: You mentioned simulation. Is that simulation tool offsetting the lack of skill sets?

Ritchey: I'm going to do a little story because it illustrates this really well. Amdahl was the first company who ever competed successfully against IBM, and I was employee number 40. We got this thing all rolled out and had a press conference. It was a big deal because it was the first computer that was all VLSI integrated circuits and the first to compete with IBM and have more power than what they had.

The press conference had a fuss about that. During the Q&A session afterward, a reporter said, "Mr. Amdahl, aren't you afraid you're making a computer so fast that it will replace thinking?" His response was, "What you don't understand is that what we have here is an exceedingly fast idiot," which is what simulation tools are. You must have the skill to run the tool. It does not replace skill. The tools never replace skill; they just let you work faster.

Whoever assembles the design team has to hire people who have the skills. There's another thing I tell my students: "If you're going to be in this business, there's good news and bad news. The good news is you don't have to do the same thing every day like the postman who finally gets so bored that he kills somebody. The bad news is that things change so fast, so you have to learn to do something new every day." It's impossible not to keep learning if you're in this business. I also tell

them that even now, I study at least one day a week because things change that fast.

Matties: Nowadays, designers need to know so much, from design rules through automation and all manufacturing. Do you think that there's so much that it's better to be a specialist these days as a designer?

Ritchey: You have to decide which part of the train you're going to get on. You have to be a specialist. DDR is getting so fast and complex that it's all one engineer can do to keep that one right without trying to do something else. My partner John's thing is DDR. The same is true of PCI Express, which is getting so fast that you can't just put things down like you're used to. There are probably more than 50 specialties.

You have to decide which part of the train you're going to get on. You have to be a specialist.

Matties: What is piquing your interest now?

Ritchey: I'm spending an awful lot of time with PCI Express because it has come to the same place where we were doing 32-GB stuff, except that was in a fairly narrow set of products. We're about to fly PCI Express on the satellite, so we can take pictures with that new telescope that is going to replace the Hubble. There's a lot of data there.

Matties: It's an exciting time when you start looking at the speeds at which data is moving. I know 5G is going to ultimately impact the general population, along with automotive, especially autonomous vehicles.

Ritchey: Automotive is one of the very toughest because of all the different things that are linked together and the environment. I can't think of any environment that is tougher than a car. Even a satellite is not that tough. You don't run a satellite through a snowstorm and a mud puddle or keep it running, park it in the desert where the inside gets to 180°F, and then go to the top of Mount Whitney where it's -40°F and gets struck by lightning.

Matties: Now that you're celebrating your "63rd anniversary of turning 18," what are some peak memorable moments in your career?

Ritchey: Probably the coolest was the first one. I was doing a radio to go to the moon right out of college. In fact, I actually have one of the prototype boards right here. I found it in my junk box, and I'd take it to class.

Matties: That must have been really exciting.

Ritchey: It was tremendous because there were no limits. It's a one-sided board. I made it at home by writing on the copper with waterproof ink and etching it with ferric chloride. Then, I drilled the holes into my kitchen table, not realizing I drilled holes on the table until my wife saw them. I didn't do any of this at home after that. But this is a prototype out of that radio, and I have the amplifier.

Matties: We just did an interview with a company that has some parts on the drone going to Mars, and the excitement of being a part of a project like that is just enormous. Back then, that must have been just incredible for you.

Ritchey: We were all spellbound. You can imagine that when the launch happened, we were spellbound waiting for that all to happen. I was sitting in my living room at 2:00 a.m., watching the landing. The irony of that is that the video did not come from any American relays because they all broke. That footage all came from an Australian relay. They were just listening in for the heck of it out in the middle of Australia.

There are more, but probably the coolest project was at Amdahl computer. We invented so many things all at once, and I actually told them when I interviewed, "You're trying to invent so many things at once that it's probably never going to work, but it will be a lot of fun." And I'll be darned if we didn't make them work.

Matties: I always appreciate our conversations so much. They're always so educational for us, and it's nice to catch up and hear your stories as well.

Ritchey: My wife calls it the "fine art of BS."

Matties: Who was it who famously said that there's only a world market of one personal PC?

Ritchey: That was actually IBM and Thomas J. Watson Sr., but the PC started out as a program for an IC tester.

Matties: Anytime you can bring a product out that empowers people's creativity, you win. That's what Apple did. I would not be a publisher but for the Apple Mac. I'm also looking at 3D and the innovation that's going to come out of 3D printing.

Ritchey: I have another little homily that I tell my students: "We have reached a point where hardware is a shipping container for software." If you want to see it in public, go on the Arista website, and every VP is listed except the VP of hardware engineering.

Matties: It has been a pleasure. Thank you so much.

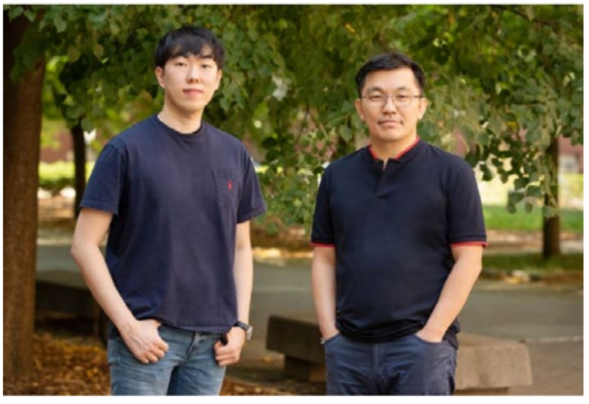
Ritchey: It's always a pleasure, Barry. **DESIGN007**

Octopus-Inspired Sucker Transfers Thin, Delicate Tissue Grafts and Biosensors

Thin tissue grafts and flexible electronics have a host of applications for wound healing, regenerative medicine and biosensing. A new device inspired by an octopus's sucker rapidly transfers delicate tissue or electronic sheets to the patient, overcoming a key barrier to clinical application, according to researchers at the University of Illinois at Urbana-Champaign and collaborators.

"A crucial aspect of tissue transplantation surgery, such as corneal tissue transplantation surgery, is surgical gripping and safe transplantation of soft tissues. However, handling these living substances remains a grand challenge because they are fragile and easily crumple when picking them up from the culture media," said study leader Hyunjoon Kong, a professor of chemical and biomolecular engineering at Illinois.

Current methods of transferring the sheets involve growing them on a temperature-sensitive soft polymer that, once transferred, shrinks and releases the thin film. Seeing the way an octopus or squid can pick up both wet and dry objects of all shapes with small pressure changes in their muscle-powered suction cups, rather than a sticky chemical adhesive, gave the researchers an idea.



They designed a manipulator made of a temperature-responsive layer of soft hydrogel attached to an electric heater. To pick up a thin sheet, the researchers gently heat the hydrogel to shrink it, then press it to the sheet and turn off the heat. Then they gently place the thin film on the target and turn the heater back on, shrinking the hydrogel and releasing the sheet.

The entire process takes about 10 seconds. Next, the researchers hope to integrate sensors into the manipulator, to further take advantage of their soft, bio-inspired design.

(Source: University of Illinois at Urbana-Champaign)

Don't Ignore DC Trace Resistance

The Pulse

by Martyn Gaudion, POLAR INSTRUMENTS

As I write this column, I just completed revising and updating one of Polar's oldest documents on impedance controlled PCBs: "An Introduction to the Design and Manufacture of Impedance Controlled PCBs with Insights into Insertion Loss." While preparing to update it, I noticed the date on the last revision was 20 years ago, in 2000.

Time flies! But the laws of physics don't. What struck me as I updated the document was how the core principles are the same, but as geometries shrink and speeds increase, the signal comes under the influence of different physical characteristics of both the copper and the laminate. This column will focus on how important it is becoming to take DC trace resistance into account when measuring and specifying thin copper traces.

A good understanding of this topic will lead to fewer spins and also reduce the risk of going down blind alleys when searching for correlation. I have noted in previous columns how, sometimes, fabricators attempt to correlate impedance before removing the effects of DC resistance from their measurements. This can lead to erroneous conclusions about the dielectric constant (Dk) if the Dk value is set by goal-seeking to make a high reading trace correlate.

All this reminds me of a conversation at IBM in France many years ago, where the engineer in charge of signal integrity joked that many SI software packages were "Logieciels comme une usine de Gaz," which literally translates to, "Software like a gas refinery." Lots of gauges and levers and pipes—and intimate knowledge of the software—is needed to get a sensible result. Fortunately, the software has become simpler to use over the years, but it remains important to remember to feed the software with good input data in order to get a sensible output.

PCB impedance control is a routine specification on many boards. As geometries shrink, fabricators making TDR impedance measurements will start to see the TDR trace rising over its length. Most of the reason for this is the DC resistance of the trace. (Note that TDR traces may rise for two primary reasons: There is DC resistance in the trace, or the impedance is actually rising because the trace is tapering.)

This DC resistance effect on the trace should not be confused with the characteristic impedance of the trace itself, which is unchanging with length. Designers should ask their PCB fabricator to use a measurement technique that de-embeds (or removes) the DC resistance from the TDR measurement.

A widely accepted technique—adopted by IPC—is launch point extrapolation (LPE). This fits a line to the TDR trace and projects it back to the start of the test coupon—the launch point—where the probe and test coupon connect (Figure 1).

Why not just test at the launch point? TDR testers used for impedance measurement look at the ratio of voltage reflected from the test trace in comparison with a calibrated 50-ohm transmission line standard. At the launch point, the reflection is masked by signal aberrations caused by the interconnect itself. For this reason, test systems make the measurement further down the line over a stable section to minimize the errors introduced by aberrations at the launch.

With line widths of four mils and above, the DC resistance in the trace is so small that the trace remains flat. As traces get progressively narrower (and with thin copper), the trace will show more and more slope, introducing an error into the characteristic impedance measurement. LPE is a proven technique to remove this artifact.

Why is the DC resistance ignored? It should not be ignored, but it is a different specification from the characteristic impedance, and the two should not be lumped together. To think of this in another way, imagine a reel of coaxial cable of 50- or 75-ohm characteristic impedance with a DC resistance of one ohm per meter. Would you say the 50-ohm cable was 60 ohms if you used 10 meters? No! the cable has a 50-ohm characteristic impedance, and the resistance per meter is a separate specification.

The same is true for PCB traces. Some PCB fabricators misunderstand this and lump the two specifications together and then try to goal-seek the Dk in a field solver to achieve a correlation between measured and modeled values. This can lead to some very odd results. If the traces are very narrow, solving for Dk

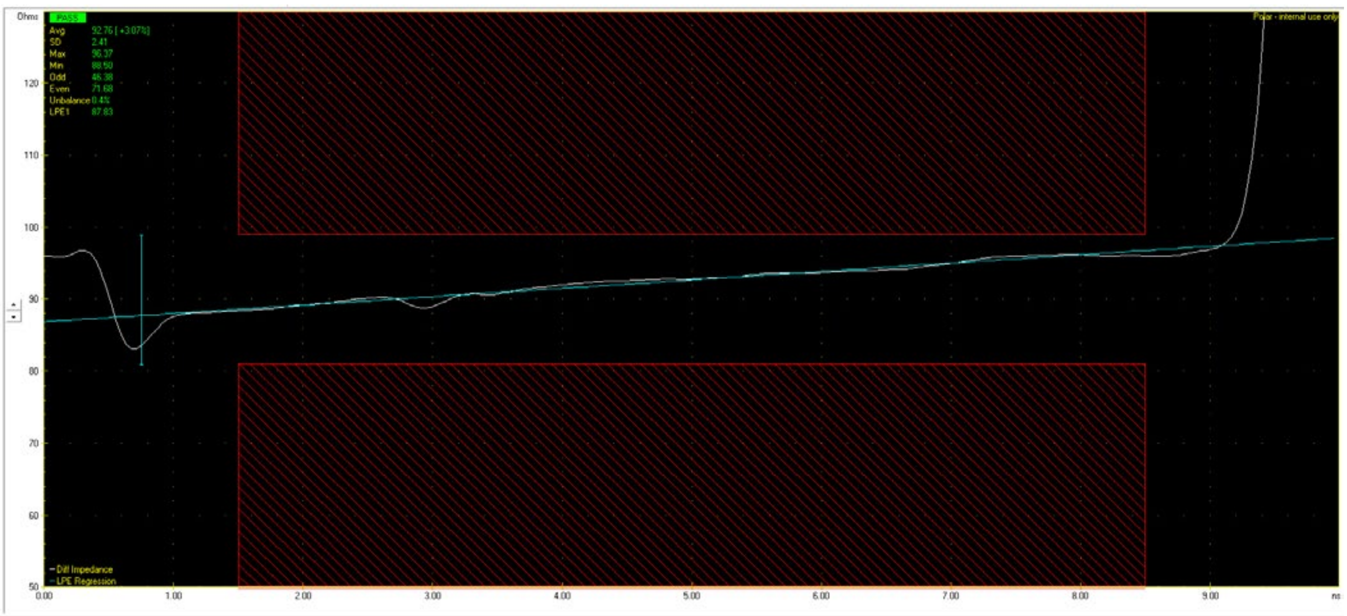


Figure 1: Launch point extrapolation.

without removing the DC resistance can lead to "that breaks the laws of physics" results where the "solved" Dk is less than that of the resin alone.

Thus, when PCB traces are narrow (approximately sub-60 microns or with very thin foils), it is imperative that a designer mandates that the PCB fabricator should use LPE or any other valid technique to remove the DC resistance artifact from the measurement before any goal-seeking of Dk takes place. Track resistance calculators are useful for gauging how many ohms per unit length should be present.

As a designer, you need to ensure that your fabricator understands the need to remove the DC resistance on fine line traces. If you have a trace designed where the resistance is 0.25 ohms per inch or more, you should specify that the impedance should be measured on a TDR using the LPE method.

To verify which is the case, simply test by launching from opposite ends. A varying impedance will rise from one end and fall from the other, and a resistive trace will show a rising trace regardless of which end the measurement is taken.

In conclusion, even though we are fortunate now that all SI software is not like the aforementioned IBM France engineer's amusing description of "Logieciels comme une usine de Gaz," even with today's simpler user interfaces, software modeling tools are only as good as the raw data you feed into them. **DESIGN007**

Martyn Gaudion is managing director of Polar Instruments Ltd. To read past columns or contact Gaudion, click here.

Sensors to Spot the Sweetest Summer Fruit

The $1.1 million Sensors for Summerfruit project launched this week by the Food Agility Cooperative Research Centre (CRC) will be led by Agriculture Victoria in collaboration with RMIT University, Summerfruit Australia and local technology firms Green Atlas and Rubens Technologies.

The three types of sensor technologies being developed and tested as part of the project will measure the sweetness of summer fruits from peaches to nectarines, plums or apricots. The sensors will be calibrated on Agriculture Victoria's Tatura SmartFarm in Goulburn Valley, and then road-tested in commercial orchards and packhouses in Goulburn Valley, Swan Hill, Cobram, and Sunraysia.

Chair of the RMIT's Cyber-Physical and Autonomous Systems Group, Professor Roberto Sabatini, said the project presented an exciting opportunity to demonstrate that the remote sensing and early diagnosis technologies they'd developed were cost-effective, impactful and scalable both within and beyond the agriculture industry.

"Cyber-physical systems, sensor networks and data fusion technologies are increasingly relying on artificial intelligence to maximise business performance, profitability and sustainability in all sectors driving the digital transformation here in Australia and globally," said Sabatini.

Research Leader Crop Physiology at Agriculture Victoria, Dr. Ian Goodwin, said the project aimed to benefit the Summerfruit sector by growing export markets and improving their operations.

"Using these sensors, we could help growers tailor their practices to grow the fruit consumers want, triaging fruit in the packing sheds, and only exporting those robust enough to make the journey," Goodwin said.

(Source: RMIT University)

Cutting Respins: Journey to the Single-spin PCB

Feature by Chris Young
THE GOEBEL COMPANY

PCB design is more than a short sprint to the finish line; it is a journey best suited for the prepared adventurer. According to a study by Lifecycle Insights, the average PCB design project requires 2.9 respins. These respins can cost anywhere from tens of thousands to millions of dollars—each!

As an engineer/business owner, I find respins frustrating because I would rather spend my time and money applying scientific principles inventing, improving technology, and solving problems. I am not an advocate for perfectionism, but rather I focus on becoming a better adventurer. Sometimes I get to taste the sweet wine that is a single spin PCB. As fellow adventurers, let's discuss some topics that influence unnecessary return trips on our PCB design journey: simulation, technical reviews, and interest in PCB design.

I like to say, "A sim in time will save dimes, especially on the assembly line." Yes, it's true: Circuit simulation guides PCB design decisions and helps avoid costly mistakes. A customer of mine ran into a simple problem of misapplying design reuse, which could have been easily caught if a simple simulation had been performed. They were using a simple NPN transistor to drive a 12V relay in a previous design and decided to use the circuit design for a new 5V design. The new product passed certification testing, and all design documents were locked down in configuration control with the regulatory authority.

The first assembly run immediately began to see failures in production testing—many more failures than were allowed by the regulatory authority. The transistor that worked well for the 12V design did not work for the new 5V design. A simple Spice simulation performed as part of the root cause analysis clearly showed the transistor did not have suf-

ficient DC current gain to drive the 5V relay. Ultimately, a respin was needed to address the issue. The cost was in the millions of dollars, and the delay was over six months.

Most often, I see respins occur due to simple design mistakes rather than some complex multiple-variable problem that exists. The lesson is that simulating your designs will reduce the risk of respins due to simple mistakes or bad assumptions.

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Peer reviews are great, but SME reviews are better. Early in my career, I fell victim to the fallacy of allowing only my peers to review my work. I was responsible for the redesign of a digital processor/IO control board in an airborne surveillance system. The control signals to the RF transmitter were TTL (5V), and my task was to interface them to an LVTTL (3.3V) FPGA. Simple enough, I thought; I will use a 3.3V-to-5V translation buffer. My peers in the preliminary design review agreed that this was a simple solution that was implemented correctly. But during system integration, an engineer noticed that when the system was powered on, a high-powered RF pulse was being transmitted from the system.

I did not understand what was happening and just happened to speak with the power supply expert on our staff. When he saw my schematics, he instantly discovered the cause of the problem. He pointed out to me that the 3.3V and 5V power supplies were not sequenced together in the design, and in fact, the 5V leads the 3.3V by several milliseconds.

During the time when the 5V is up and the 3.3V is off (~0V), the 5V transmitter control signals from the translation buffer are commanding the transmitter to transmit at full power. This resulted in a respin of the processor/IO control and power supply boards in the system. Including our power supply expert in my design review would have avoided two board respins in this project. Lesson learned: Always include subject matter experts in your design reviews. They have valuable knowledge and insights that can help keep you out of trouble.

Respins do not have to be a part of your company's reality. If you enjoy PCB design, invest your time in becoming good at your job. Being interested in PCB design gives you the tenacity needed when facing difficult or complex design problems, and it provides the fuel for improving your design skills.

A litmus test for gauging your interest in PCB design is how you spend your free time. Do you find yourself daydreaming about PCB design in your off time and/or tinkering at home with your own designs?

If the answer is yes, then I suggest you find others who enjoy it as well, including SMEs from across the PCB design spectrum. Interacting with those who share your interest in PCB design helps strengthen your own abilities. An excellent resource for connecting to others with strong interest in PCB design is the Printed Circuit Engineering Association. PCEA's core values of collaboration, inspiration, and education are derived from the founding members' expertise and interest in PCB design. My inspiration for sharing my ideas and experiences in this article is derived from my interest in PCB design and encouragement from like-minded colleagues and friends.

Remember: A sim in time will save dimes. And always let the appropriate subject matter experts take part in your design reviews. You might save your company millions of dollars and months of lost time-to-market. **DESIGN007**

Chris Young is chief hardware engineer for The Goebel Company and owner and lead engineer with Young Engineering Services.

To Coat or Encapsulate:

Making An Informed Choice for Electronics Protection

Sensible Design

by Phil Kinner, ELECTROLUBE

One of the most frequently asked questions we receive from customers is, "Which is better to protect my PCB: a coating or a resin?" PCBs are found in many domestic, industrial, automotive, and military devices and require protection from their environment. Lack of protection can lead to reduced performance or, in the worst case, a complete failure. Protection can be offered in the form of conformal coatings or potting and encapsulation resins.

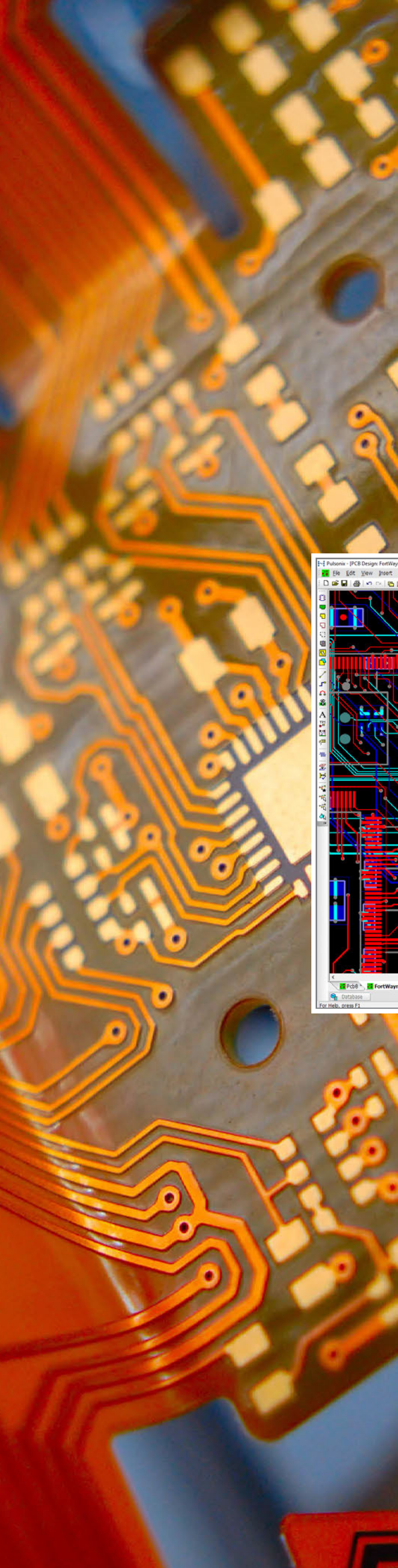
In this month's column, I will demystify why one may be more suitable for your application than the other. Like any good engineering answer, it depends on the degree of environmental protection required. The first point for consideration is often the design of any housing within which the PCB will be enclosed. If an assembly is enclosed in a housing that is designed to be the primary environmental protection, then a conformal coating is often used to provide a back-up to the primary protection provided by the housing. Where the housing is not suitable or capable of providing primary protection of the assembly from its operating environment, then most times, a resin might be a better choice.

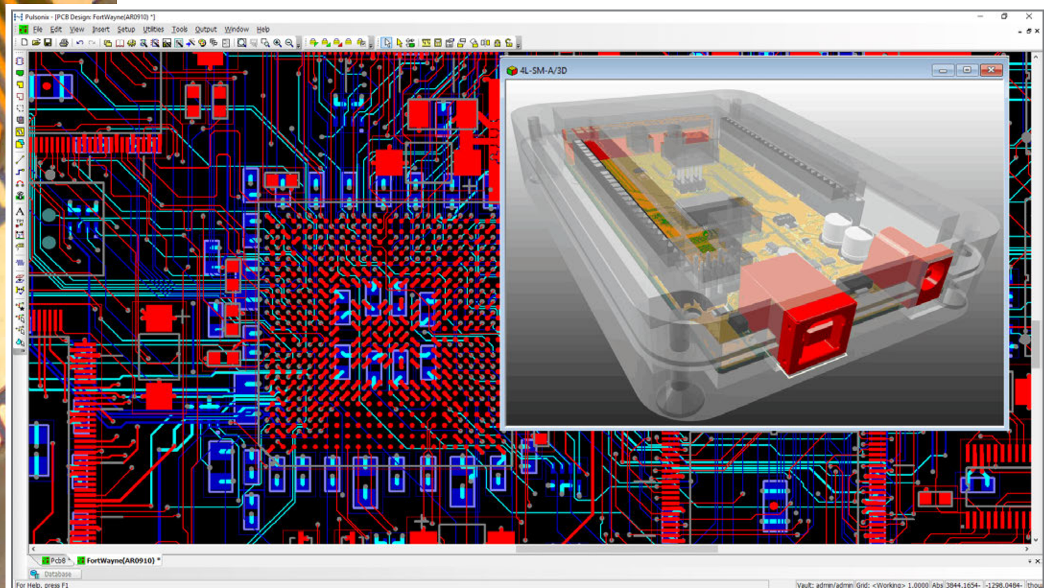
If we look at both coatings and resins, then we can consider what is common between the two. Both are generally organic polymers, which can cure to form an electrically insulating layer that provides some degree of chemical and thermal resistance. There is a degree in commonality in the chemistry of the polymers used, with acrylic, epoxy, polyurethane, and silicone being the most often encountered.

Without further ado, let's explore coatings and resins in more detail in our five-point format.

1. What is an encapsulation resin?

Potting and encapsulation resins offer the highest level of protection for PCBs. Resins can be applied from 0.5 millimetres upwards





and are generally applied much thicker than this. The increased thickness leads to a significant increase in weight and often results in a greater per-unit price than a coating. However, the increased thickness does mean that the PCB is far better protected against chemical attack, particularly in the cases of prolonged immersion.

Also, a resin can provide superior protection against physical shock (depending upon the formulation) since the bulk of the resin will help to dissipate the forces. A layer of dark-coloured resin can also completely hide the PCB, which allows for some security of the design. Depending on the choice of the resin, removal of the resin can also result in the destruction of the PCB. With so many varying options to protect electronic circuitry, there's a lot of ground to cover, and depending on the application, sometimes a conformal coating may be more suitable—particularly with the two-part coating series that performs like a resin.

2. What is a conformal coating?

Conformal coatings can be used to protect the PCBs in a variety of applications, ensuring optimum performance in the harshest of conditions. They are generally thin films applied in the 25–250-micron dry film thickness range, leading to a minimal weight increase of the assembly. Conformal coatings conform to the contours of the board, providing maximum protection with minimal weight or dimensional change to the PCB. This is possibly the primary advantage of conformal coatings over potting and encapsulation resins.

Often, coatings are clear, so the coated components are easy to identify, and the coating can be easily reworked and components replaced as required. The chemical and thermal resistance of coatings is generally good for short exposures. A coating applies relatively little stress upon the components. This is a particular advantage where a component has thin leads or legs. The majority of coatings are 1K (single-component) systems, which have a long useable life, a low curing or drying temperature, and short drying time.

Being a single-part solution, they are clearly easier to process and apply; however, the majority of 1K coatings are solvent based in order to modify their viscosity for application purposes. Conventionally, coatings can be applied manually by use of a paintbrush, spray gun, or even manually dipped. Increasingly, however, coatings are applied by robotic selective coating systems to provide a more controlled and more consistent process.

3. Is it possible that a conformal coating can perform like a resin?

To confuse matters further, the simple answer to this is yes! We've developed a wide range of two-part (2K) conformal coatings, which combine the protection and properties of a resin with the ease of application of a conformal coating but without the use of solvents, giving them an environmental advantage. The 2K coatings provide excellent coverage, and their superior flexibility offers protection of delicate components.

2K coatings also deliver excellent mechanical properties and abrasion resistance, but, being two-part, they require more sophisticated application equipment than 1K coatings, and they are more difficult to remove, making board repair more difficult. Based on similar two-part chemistry to resins, 2K coatings are designed to be applied by selective coating equipment in the range of 200–400 microns (0.2–0.4 millimetres), combining many of the advantages of both technologies and minimising many of the drawbacks of each.

4. What are some key differences between resins and coatings?

The most noticeable differences are the methods of application (aerosol, conformal coating spray equipment, manual spray gun, and brushing for coatings, compared to mixing and dispensing equipment and resin packs for resins). The materials are applied at different thicknesses (< 100 microns for conformal coatings, < 500 microns for 1% solids coatings, and > 500 microns for resins). Coatings are generally approved to international standards (IEC-1086), military standards (MIL-I-46058C), industry standards (IPC-CC-830), or national safety standards (UL746), while for resins, it is very much dependent on the application, and there are very few standards.

Due to the coating thickness, coatings occupy less volume and have a lower increase in overall weight compared to resins. There are both coatings and resins that are based on epoxy, polyurethane, and silicone chemistries, but there are also acrylate, acrylic, and parylene coatings that do not have a direct resin equivalent. Ninety-nine percent of resins are 100% solid systems, so they have low or no VOCs released during curing, while many coatings are high in solvent content, although there are two-component (2K) and UV-curable acrylate systems that are also available as 100% solids.

5. Why would I choose a resin instead of a coating?

Fundamentally, the choice will often depend on the design of the housing. If the housing is designed to be the primary protection, then a coating will often be used to provide secondary protection or additional insulation. If the housing is not the primary barrier to the environment, then an encapsulation resin will often be used to augment or replace the housing.

The choice between a resin or a coating normally comes down to application specifics. If the unit involved is to be subject to long-term immersion in various chemicals or subject to long-term thermal and/or physical shock cycling, then a resin is generally preferred. Also, if there are a large number of large components on a PCB, it is sometimes better to use a resin to encapsulate these than to coat them. Another scenario where a resin would be preferable is when the unit will be used in a situation where it is not easily accessible, or a long continuous service life is required. In this case, a resin would be recommended to provide the extra protection and durability needed.

However, the 2K conformal coatings have demonstrated excellent performance in condensing environments and immersion tests. In recent trials simulating highly condensing and immersion conditions, a urethane coating, 2K301, gave the highest overall values in terms of circuit protection and showed the least change during condensing/immersion events. The very large difference in thickness between the 2K conformal coating and a urethane resin potted assembly didn't show a large increase in performance.

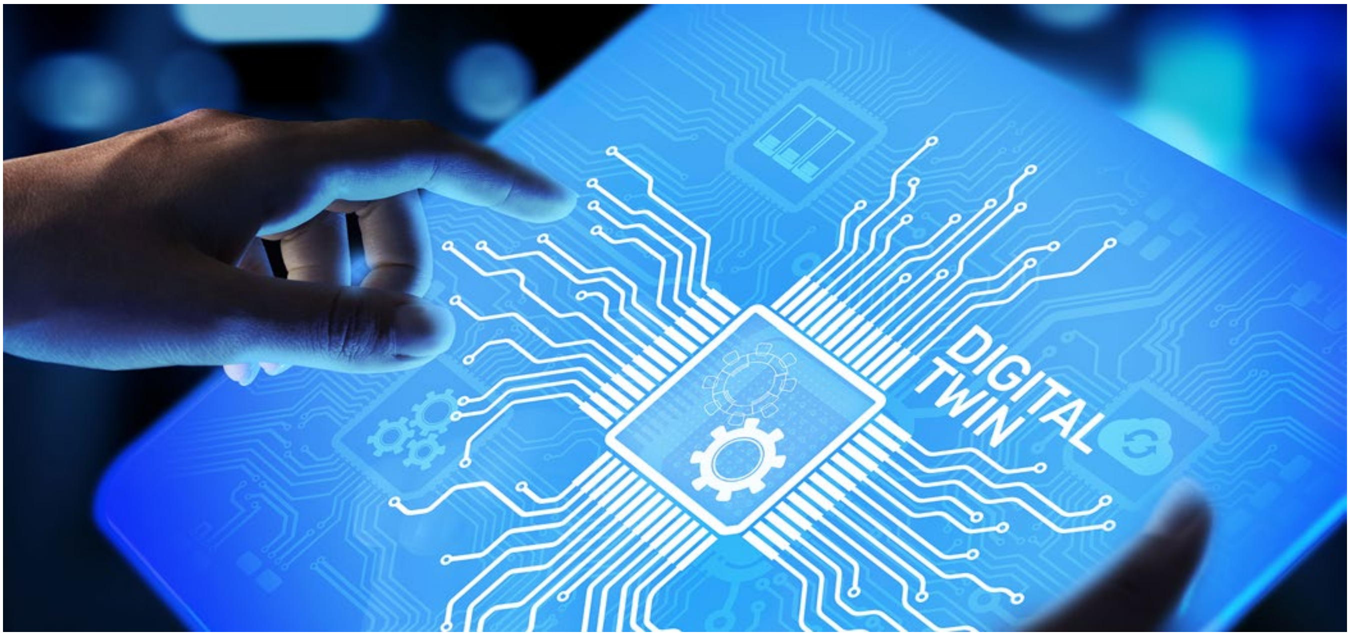
Indeed, the 2K coating achieved much the same results as the resin applied at one-tenth of the thickness. 2K conformal coatings can be applied more thickly than previous coating technologies without the risk of cracking. They can also be readily applied by selective coating techniques to provide a coating with better thickness and sharp edge coverage that has performance somewhere between where a conventional conformal coating fails and potting is required.

Conclusion

Every customer and their project is different. Whilst we can advise a customer as to which products are best suited to their needs, based on our years of experience, it all boils down to the unit, the environment it will be subjected to, the dispensing method/equipment to be used, the curing times, and the temperature limitations that may be imposed during the production process. The more information that a customer can provide regarding the ultimate operating conditions—temperature range, likely chemical exposures, and so on—then all the better.

Look out for my next column, where I will look at more considerations to improve the lifetime and reliability of electronic assemblies. **DESIGN007**

Phil Kinner is the global business and technical director of conformal coatings at Electrolube. To read past columns or contact Kinner, click here. Download your free copy of Electrolube's book, *The Printed Circuit Assembler's Guide to... Conformal Coatings for Harsh Environments*, and watch the micro webinar series "Coatings Uncoated!"



There's No Excuse for Bad DFM Practices

Feature Interview by the I-Connect007 Editorial Team

Happy Holden and Michael Ford discuss the need for new approaches to bridging the gap between design and manufacturing. Michael explains why the combination of IPC-2581 and CFX means there is really no excuse for designing boards that are not optimized for your fabricators' processes. As Michael says, now's the time to break down barriers and really drive DFM—and the industry—forward.

Andy Shaughnessy: We're here to talk about DFM and what we can do to help designers and CAM engineers who keep receiving incorrect data. Why does DFM seem to be "a bridge too far?"

Michael Ford: There is a very large gap between design and manufacturing, and it comes from three different things. First of all, there is distance. Manufacturing is quite remote from where the design is done. As well as distance, there is also the separation of time, as manufacturing can happen months later, after the design is completed—by which time, the designer will have moved on to other projects.

But it's also about the different technology domains. When you have a problem in manufacturing, the manufacturing person starts talking about attributes of their pick-and-place and reflow oven profiles, for example, which is a language that the designer simply cannot understand.

Each side is very much focused on their own experience and technology and the way they describe things, and there's little that actually meets in the middle. Because manufacturing is so complex, with many different machines and materials, it has been very difficult for anyone to get that information successfully across.

Happy Holden: One of the things I tried to teach my design engineers that were doing board layout—even though they could see multilayers being made in the same facility—was that "you have a big job learning how to design PCBs with keeping a schedule, EDA tools, new components all the time, shrinking rise times, and thermal issues. It's everything you could do to be the world's best PCB designer. I don't expect you to be manufacturing experts. The only thing you should do is take a tour of the shop and walk away with the concept that fabricating a PCB is complicated. If a ques-

tion comes up, send an email or walk down the hallway and ask manufacturing. I can't expect you to be a manufacturing expert."

One of the big problems is that there's never been a detailed diagram of how a PCB is designed. At some point, you have critical questions about placement, layout, and all these different things that can go wrong. We would then take these questions over to the CAM people and say, "Provide an answer for these things and normalize it in terms of the cost of the final PCB." These different choices had costs associated with which ones were cheaper than other ones.

Michael Ford

Then, we'll write that and put it into a table or a check sheet for designers. If they hit that point, they could at least get some indication of the ramifications of the choices they have to make. I've never seen that in any book, design course, or IPC standard. If there's an infinite number of ways of laying out a PCB, how do you choose the optimal path? What if I placed this CPU close to the edge where I could only route out at three sides instead of four sides?

Ford: The outlook is a positive one, as there have been some interesting recent developments. A couple of specific things have happened. First of all, revision C of the IPC-2581 standard, now called DPMX, is imminently about to be published. Revision C has a new module within it, specifically for DFM feedback. Now, this is not the old-style, rules-based DFM, which is basically a design rule check with just a few more rules that have been introduced from a manufacturing perspective; it is a mechanism through which designers and manufacturers can directly communicate in a defined, digital way. Instead of sending a multitude of documents and drawings, having phone calls, and exchanging emails—all of which can easily get lost or be misinterpreted—there is one channel through which all of the information flows.

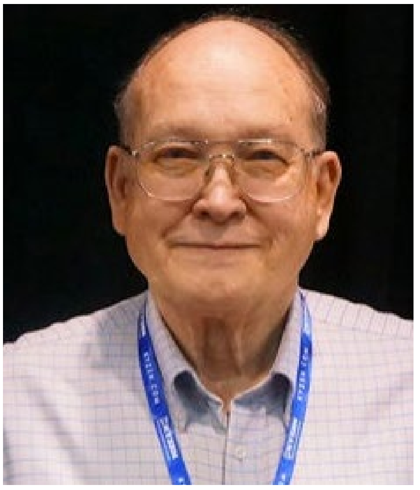
The second interesting thing to happen is that the DPMX file (i.e., IPC-2581) is now starting to be used in assembly manufacturing itself. Previously, design data would flow primarily into a digital manufacturing engineering system, which would calculate all of the different pieces of data required for each of the machines, as well as applying the local BOM. When it came to machine programming, however, the machines would need more information about the design of the product. To address this, the IPC Connected Factory Exchange (CFX) IIoT data exchange features the ability to send the original IPC-2581 file to the machine directly so that the whole of the design data can be immediately and accurately referenced. We're going to see a couple of press releases in the very near future where the most advanced machine vendors are actually already adopting this.

Holden: That's kind of like a TAM network.

Ford: Yes. The problem has always been that the design information itself has been difficult for the different domains to fully understand. The IPC Digital Twin, as has recently been defined, architects how information should be made available across disparate domains. Information from different processes is resolved down to the digitally understandable content, such as what you get from a DPMX file. This is now one part of the overall digital twin. It's the connection and interoperability that the design and manufacturing world needs.

Nolan Johnson: Does this start to set up the opportunity for CAD tools and fabricators to talk more real-time or interactively as the design progresses?

Ford: It's the first stage. What we would like to see with the designer is instead of being project-based with a cut-off before the product is introduced into manufacturing, they work together with manufacturing, where there's a continuous flow of information between the two. As manufacturing is usually remote from design, things happen—such as material shortages or pricing issues—that invoke alternative materials from local suppliers to be chosen, for example. Manufacturing often uses materials that the designer did not authorize or even foresee. All of your DFM rules in the world would not have included logic about exceptions that happen beyond the control of the design.



Happy Holden

Therefore, there needs to be a collaborative platform on which the local manufacturer, looking to source alternative materials that will satisfy the need of production in this instance, would seek and get permission to make the substitution from the designer, who will respond to confirm that the functionality, specification, and physical attributes—including the leads, pads, shapes, and size, etc.—all look good. This process doesn't happen today, or if it does, it's extremely ineffective, as such interactions occur too late, and the designer has moved on to something else.

Holden: That's important because we have engineers who pick a component and everything seems okay, but if they ask the assembly test people, they would say, "No, we have a lot of failure and test issues with that component. This component over here does the same thing but has a much higher quality testability level than what you selected."

Ford: That is often the case and may be a localized issue. It may depend on certain production equipment, as well as material vendors. It's really important to have interaction. I've seen that kind of feedback work very well, where instead of the legacy DFM problems I mentioned earlier, the manufacturer can show information, such as when you use this component, there is a first-pass yield issue of around 100 ppm; however, if you were to relocate or site that component with a different orientation, the first-pass yield defect reduces to 10 ppm. That form of information is very easy for designers to understand because the whole issue of domain-based technical language has been eliminated through the use of data.

Johnson: That sounds like a huge amount of data being turned into statistical AI recommendations that can be fed back. It must mean a huge change in what the manufacturers are collecting for data, how they're presenting it, and a great deal of AI and knowledge-based expertise going to the fabricators.

Ford: The focus of a lot of people in manufacturing right now is to collect as much data as possible; in most cases, they collect messages from machines. The IPC CFX standard is the most efficient way to collect the data from machines, but context is needed to create values.

Qualified facts and events should be communicated, but if you only exchange the raw data—which would incidentally be massive in terms of data size and complexity—how is the designer supposed to understand it? Any design-based computer software has a similar problem; in the same way, a human designer can't understand the manufacturing engineer, the designer's computer solution can't understand the manufacturing data. Contextualization of many data points together at the manufacturing side creates meaning for others to understand. We also have to eliminate all internal causes of variation that occur in manufacturing so as not to confuse contributions to the root cause. We then have the basis of factual feedback to designers and their systems in a way that they can understand.

Johnson: Historically, it has been the situation where you would write that up as a rule deck. In IC, in the early days at Mentor Graphics with Calibre and xCalibre, for example, one of the things that the product team did was to work with the semiconductor fabs to create rule decks that captured a particular process. It was a static thing. That's where we've been in PCB when it comes to DFM up until now; it has been a static set of rule decks.

Ford: Exactly, there are two problems with rule decks. One is that they're never accurate because manufacturing technologies continue to evolve. The second thing is the rules become so complicated that nobody can understand or remember how to keep them updated. We have to find something which is more meaningful yet simple. We have to find the specific language that we would use to exchange data from manufacturing and design, which is exactly what has been defined within the IPC-2581 standard. It's a really exciting project.

Holden: The other problem with rule decks is that they are a slope. In other words, make it robust and large, and it's easy, quick, and cheap. When you get toward the limit of technology, it becomes long, expensive, and complicated. Where do you put this rule, and where do you set the thing down on the rule? Most things don't accept rules as "it depends."

Ford: Definitely. People never seem to agree on what those rules are. They will always want it to be a little different because their conditions are different, perhaps unique. What we would really like to see, however, is the common platform on which all perspectives sit, such that each solution remains interoperable. This has been the intent of the IPC Digital Twin. We've all seen digital twin-based solutions being advertised. Everybody is claiming a "digital twin" these days in some form as part of their solutions.

The problem with solution-based digital twins is that they are all bound by the extent of their solutions. Within the proprietary bubble, they can do anything they like, but they cannot address or utilize anything beyond. Their contextualization is limited because if you cannot qualify events or changes that are triggered outside of the bubble, then how can you take those factors into account? For example, if you measure deviations in X and Y of component placements on a PCB relative to the surface of the board using the AOI machine, but you didn't see the fact that the batch of the PCBs has changed, which brings with it a new set of variances, how does that impact your statistical analysis of the trend that you see for placement accuracy?

Johnson: How are the EDA vendors responding to this moment in time?

Ford: They're extremely positive. The IPC-2581 committee is made up of a lot of these key design software vendors. The breakdown of these artificial barriers to interoperability is driving the industry forward. One of the great examples that I saw, getting back to assembly with CFX, is that you had the scenario before where individual machine vendors had their own flavors and formats of data, and nobody could understand anything from anyone else. Suddenly, four years ago, all of the machine vendors sat down together in an IPC meeting and said, "We need to share production information with our customers in an easier way. Machine vendor IP isn't contained in the data or its format; it is actually how the machine is designed. We want to have now data interoperability."

Johnson: Andy, what Michael just said lines up with the "a-ha moment" we had yesterday. A marketing director at Altium made the comment that designers used to have a year to work on a power amplifier, and now designers are doing multiple designs in a month. There was plenty of time to stew on it and to think of the subtleties and the nuances in your design. If you're doing two a month, you just don't have that.

Holden: Michael used the right word: collaborative. What we need and what IPC-2581C and future revisions are pointing to is kind of the Zoom screen for collaborative design in which you have electronics layout, including signal

integrity, thermal, fabrication, assembly, and test. We are all sharing fundamentally the same information and coming up with ideas and solutions that all can agree to, or one of us says, "I have a problem with that because of this," but the next person says, "We can solve that problem with this." You've quickly collaborated, and you don't make the mistake of jumping down the deep well that later requires a re-spin.

Ford: The nice thing about this is that it's not just product-based. You can break down any product into modular components. You could have a small module of circuitry, which could be, for example, a power supply, perhaps an interface. The whole design can be broken into these modular components. You can even break down the modular components further into specific features, whether based on, for example, the shape of a land pattern, a type of component, or even specific reference designators. You can get into as much detail you like. You can talk about the success or otherwise of those features in different processes. When you come to making a new design, you have all of the associated information about layout and component decisions that you're making at your fingertips ahead of any prototyping stage.

The nice thing about this is that it's not just product-based. You can break down any product into modular components.

Holden: It's much easier for AI software to look at those solutions and come up with generalized models based on a lot of different things that the human wouldn't have time or inclination to figure out what's common with this and what's not common.

Ford: Human intelligence (HI) is the best form of intelligence, but it's also the laziest (laughs). Artificial intelligence (AI) isn't yet quite so good creatively, as it's just a sequence of algorithms, but it's dogged. AI will quickly spend billions of computing cycles, finding the very best solution to a problem or task. The vast majority of work in the digital world is a repetitive application of rules associated with any problem. AI can, therefore, be very effective at providing that first-off context of things and handing it over to the HI to do the final stages. We will see an increasing trend in that direction almost everywhere.

Shaughnessy: Does all of this fit under the umbrella of predictive engineering?

Holden: What I was saying was predictive. Other people were calling DFM and design rule checking, which is after the fact. I'm back to Dewhurst and Boothroyd: As we do the design, let's predict the problem and solve it so that it does not become a problem.

Ford: It is all about prediction, though that is a difficult word because people often associate it with long-term simulation. Taking a product, a production line, and certain tasks to be done, let's simulate and optimize how things are going to happen. There is some established software to do this that will come up with an excellent solution. Two days later, however, the production situation changes, the simulation criteria are now obsolete, and you have to start the simulation again. Any form of prediction and optimization has to happen much faster now, in near real-time, using information that can be derived about every facet of the situation. It's a new digital world, and this feeds very nicely into smart factories and Industry 4.0 because this rapid response flexibility is exactly what those concepts are driving.

Shaughnessy: What has to happen to make this a reality? Is this going to be led by the EDA vendors or the designers?

Ford: There are a few different stages. At first, there needs to be an understanding of the value of interoperability. We need to create the motivation behind it, as it's not really going to work if just one domain thinks it's a great idea, but the other doesn't. Designers, manufacturers, and all of the different components across the whole life cycle of the production-related business need to be on board and say, "I see the value of data. I want to be a part of this interoperability. My solution is much better now because it has interoperability," so they can realize the benefits.

We use the technology that IPC has established with DPMX with CFX, together with the IPC Digital Twin, in particular, to enable collaboration in a way that benefits everyone without running into competitive issues. We saw this happen with CFX; all machine vendors, customers, and solution providers are benefiting, so we expect the same to happen elsewhere.

Holden: The best way to drive this is going to be from the OEM perspective. The OEM is the big winner on this, which means that once they believe in it, they find their favorite software vendor who seems to be best capable of writing the software that's interoperable and collaborative and put that software together for them with the caveat that you can't release it to the market for at least a year.

Ford: I completely agree with that. There are people out there who are already looking for this. The nice thing about working in the standards organization within IPC is that you get to see the start of these things happen. The business owner of the product is at both ends of the business process; they're doing the product design, and they're also monitoring the product reliability in the market. They can see the whole picture, and for them to be driving this process is perfect.

Holden: You finally reached the level of HP software 1998 because this is what we called Order Express version three, which did this all in X windows, things like that. Again, we never let Valor see it, so there was no way they could come up with a product, but it was all because of standardization. That was a vital part of our schematic to finish a prototype in five working days, which we achieved in five and a half days.

Ford: Exactly. That's a great result, and it shows that it can be done, even years ago. We have new tools now, making life easier, so we have no excuse. We're doing it on a slightly bigger scale, as we want the whole industry to get on board with it, but you've shown that it can be done.

As we come out of the COVID-19 pandemic, as well as other things going on in the world, we have to be on our A-game. We have to be ready to take the challenge of how we're going to expand and recover business and be differentiated and successful, and that's going to be based on very fast reaction times in both design and manufacturing, with the ability to quickly make strategic decisions.

Johnson: That's a good point and begs the question, "How does a design team move this along?" because they're going to be a big benefactor from this.

Ford: It's interesting in the OEM world. When manufacturing is being done in-house, there is easy and direct feedback. You can change things and justify it based on the nature of the results that you expected to see for the product in the market. When you get into the EMS world, it's a little bit more difficult because you

have specific contracts and differing business interests. EMS companies do different things for many different clients, though they don't want to have 20 different ways to do the same thing; in reality, this is often the case.

Applying standards to EMS companies may seem a lot more complex than on an OEM basis, but ultimately, having common methods for interoperability will give the EMS side the greatest benefits. Influence needs to be there now in terms of setting expectations. Everyone needs to understand that the option is there to continue to work separately and pay the costs and consequences of things as they go wrong, or we can work together in a digitally interoperable environment, and all be more profitable.

Holden: We used to call that concurrent engineering, but collaborative engineering may be a better word. Are you on the IPC-2581 committee?

Ford: Not directly. I work with people on the communications and marketing side of the associated DPMX consortium. The DPMX revision C press release is about to go out. There are others that are related in the pipeline coming from machine vendors, one very imminently, for the use of DPMX within manufacturing. Then, there's the publication of the first release of the IPC Digital Twin. There's a lot going on!

Holden: Will you set something up for IPC APEX EXPO 2021?

Ford: Absolutely. I know we're planning something for the IPC Digital Twin, within which DPMX should also be highlighted. There will be a whole series of discussions I expect about what's new in revision C, especially within this DFM area.

Holden: Where do you think we'll see the first prototype software or something like that? Will it come from EDA vendors, machine vendors, or third-party companies?

Ford: As we are talking about an interoperable environment, it's going to be all three together to some extent. The ideal condition takes place where you have a factory, and all of the machines are talking through CFX. IIoT-enabled MES software is collecting the data and creating contextualization. Fully qualified information is then available to whoever wants to use the data to create value. Until that happens, software in other domains couldn't even start to be developed. As we're collecting the data, algorithms are being further developed to make sense of it and use it for many potential values.

In parallel, you will see a similar situation developing between machine vendors, who are both consuming data as well as creating it, and companies that are creating the overall contextualization. Standards are there to promote this process and push it forward by creating communication technology, but they are not the solutions in themselves. We always ensure separation of the work on standards, which creates a level playing field for many different companies to contribute to as well as to utilize, and the resultant commercial solutions themselves.

Shaughnessy: Thank you, Michael. It has been great having you discuss this.

Ford: My pleasure. I hope to see you all in person soon! **DESIGN007**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PCEA 2020: Small Rearview Mirror, Big Windshield

The Digital Layout

by Kelly Dack, CIT, CID+, PCEA

Introduction

In this month's forward-driving column, I glance back at PCEA's year in "rearview," which included an energetic jump-start, some challenging air filter retro-fitting, some remote diagnostics, and a final refueling at a very successful virtual chapter meeting. Next, I hit cruise control and rely on PCEA Chairman Stephen Chavez, who focuses on what lies ahead between the vanishing points of highways 2020 and 2021. As always, I'll also point out some interesting events for you to consider attending.

PCEA Updates

There are many good metaphors based on cars and driving. A recent one regarding the past year resonates with me by pointing out the differences in size between a rearview mirror and a windshield. You only need to glance in the rearview when backing up or trying to see what may be overtaking you. But if you're driving forward, your main focus should be on the large, clear windshield to see what's coming.

2020 was a great year for the PCEA. It had to be because it's the only one we've had. We were started by a group of designers, engineers, and PCB industry representatives and professionals who found themselves looking for a new set of wheels after the dissolution of the IPC Designer's Council and its executive staff in November 2019. The group was not ready to hang up their passion for highlighting and representing PCB designers. Additionally, they acknowledged that there needs to be a more intimate organizational structure to better cultivate and grow relationships with

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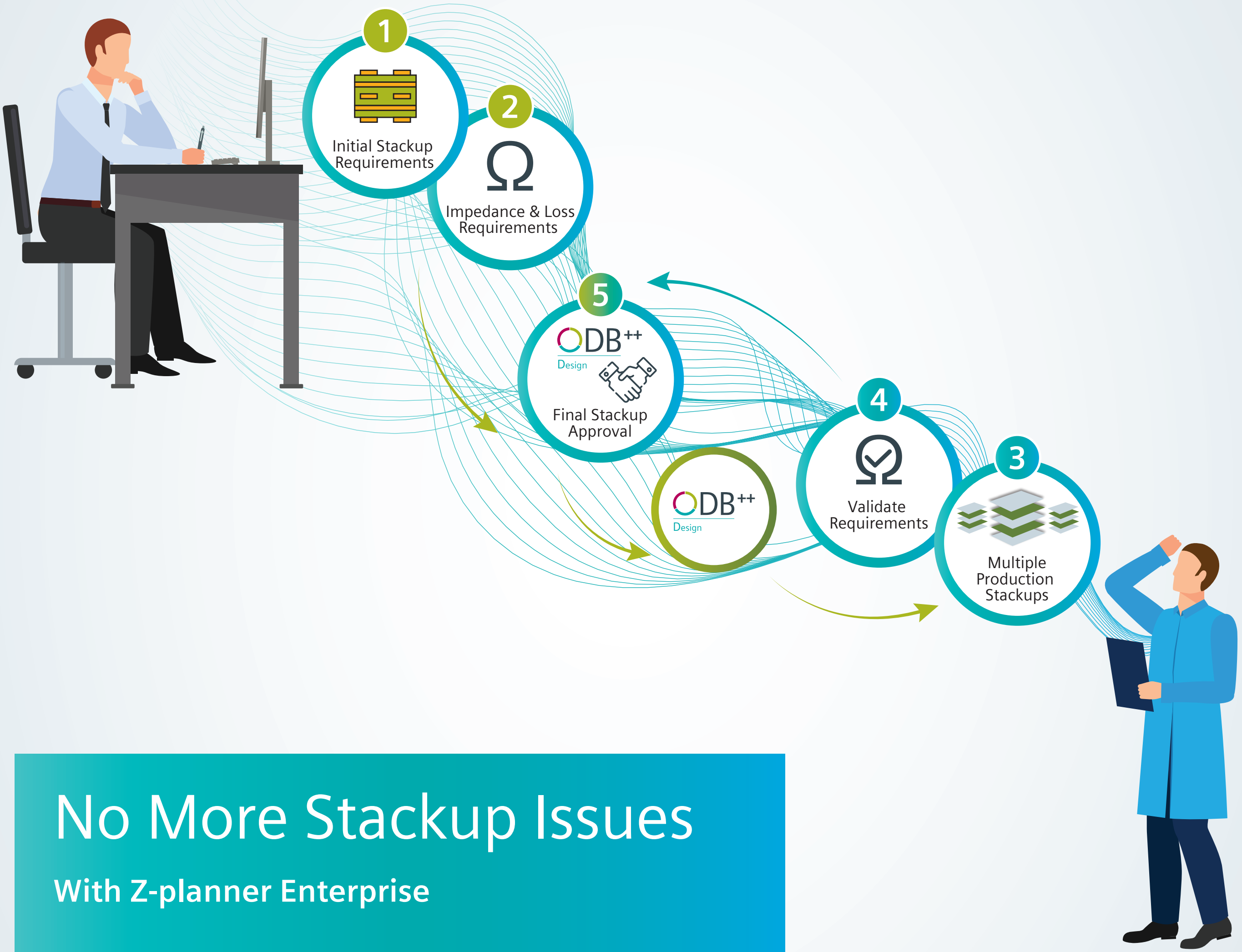

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all vital stakeholders to understand and communicate each other's requirements during the vital phases of design, manufacturing, procurement, and test.

In January, meetings were called, and the group came together to prepare the vision and restart as a grass-roots organization with a mission to collaborate, educate, and inspire the electronic industry to create better printed circuits. However, the group members soon found themselves masked and quarantined with virtually the rest of the electronics industry. Meeting over the past months, the group managed to incorporate as a nonprofit after forging the PCEA. The monthly column was established a few years ago by Stephen Chavez, who delegated it to me after he was named chairman of the PCEA.

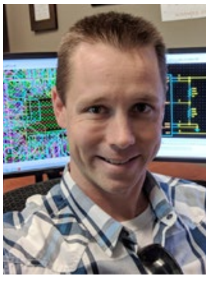
In less than a year, the foundation of the PCEA was laid. The organization held its grand opening event online, touting over 1,000 members with many local chapters itching to meet again. More recently, the San Diego, California, and Phoenix, Arizona, chapters hosted a successful virtual chapter meeting attended by over 50 industry professionals from all over North America, including Canada.

October PCEA Chapter Meeting

Local chapter presidents Luke Hausherr (San Diego Chapter) and Randy Kumagai (Phoenix Chapter) kicked off the meeting on October 28 with greetings and an introduction to PCEA Chairman Stephen Chavez. Steph gave an overview and called on people to spread the word that the PCEA is ready to fulfill its mission of leadership, membership, and continually growing industry sponsorship. One recent sponsor, Insulectro, delivered a technical session on design innovation related to PCB materials, which was given by VP of Technology Chris Hunrath and Technical Director of Design Education Mike Creeden, who is also the PCEA's vice-chairman.

Mike Creeden

Chris Hunrath



Luke Hausherr

Topics covered included:

- Design innovation
- Hybrid stackup models
- Material properties and considerations
- Effects of loss tangent
- Mixing laminates
- Embedded capacitance
- Advanced HDI structures

After the presentation, the chapters hosted a raffle with some outstanding prizes. Luke selected the winners. The grand prize was a seat of PCB Library Expert, which was thoughtfully provided by PCB Libraries.

Message From the Chairman

by Stephen Chavez, MIT, CID+

Stephen Chavez

What a year! Most of us will never forget 2020. With all that is going on in the world today, it amazes me how many have adapted to the virtual world, didn't break stride in meeting today's challenges, and continued to be successful. Our industry's evolution waits for no one, and many have stepped up to the challenge and conquered it. When I think about how 2020 unfolded for the PCEA, we have far exceeded our initial expectations and goals for the year.

From our grand opening back on July 14, our membership continues to see very strong growth month after month. We are not only having growth from within the U.S., but we also have international growth. Our local and regional PCEA chapters have seen momentum and success. We now have 10 active domestic and international chapters, with eight chapters at their infancy stages and many others coming soon.

What excites me most about the chapter activities is how each of the chapters is collaborating together and functioning as one collective for the better of the industry. For those of us who have been around for many years now, and actively involved within the industry, this type of chapter to chapter communication and activity has not been seen before. We truly have collaboration, inspiration, and education taking place, especially within our chapters from one virtual event to another. There is an exciting buzz within the industry about the PCEA.

If membership and chapter growth, along with activities, aren't exciting enough to make you want to join the collective, then our industry affiliation and collaboration both domestic and internationally will inspire you, which is seeing the same type of growth. Our sponsorship also continues to make strides as we continue to get lots of positive feedback and buy-in to what the PCEA is all about. And there are still lots of free webinars out there, so take advantage of them as you can.

Our future looks extremely bright. For 2021, look to see more activities, collaboration, and synergy between all PCEA chapters. You'll also see growth with our industry affiliates and sponsors to solidify our mission to collaborate, inspire, and educate. The year will be even better.

If you have not yet joined the collective, I highly encourage you to visit our website at PCE-A.org and become a member.

I continue to wish everyone and their families to be healthy and to be safe, and much success in 2021.

Next Month

As our leader Steph is doing his job to set the vision, the PCEA executive staff will be meeting again soon. We will be taking feedback from our local chapters and working with our sponsors to make concrete plans for PCEA events to help this industry to connect and become more educated. I will report on the materialization of these evolving plans in our first column of 2021, so stay tuned.

Upcoming Events

- March 6–11: **IPC APEX EXPO** (San Diego, California)
- April 13–15, 2021: **DesignCon** (Santa Clara, California)
- May 11–13, 2021: **IPC High-Reliability Forum 2021** (Baltimore, Maryland)
- November 10, 2021: **PCB Carolina** (Raleigh, North Carolina)

Spread the word. If you have a significant electronics industry event that you would like to announce, please send me the details at kelly.dack.pcea@gmail.com, and we will consider adding it to the list.

Conclusion

It's sometimes a relief to look back through your rearview mirror and clearly see what you've left behind. But through a dirty windshield, covered with COVID-19 and other challenges, it can be daunting to drive forward without vision. At the PCEA, we want to be the windshield wipers or the sponge and squeegee to help you wipe your printed circuit engineering apprehensions away. Our collective will help you see where your industry is going and inspire you to take the wheel, hit the gas, and enjoy the ride. Now is a great time to check us out at PCE-A.org and make a New Year's resolution to rideshare with us. We're in it for the long haul and have lots of experienced designated drivers.

See you next month or sooner! **DESIGN007**

Kelly Dack, CIT, CID+, is the communication officer for the Printed Circuit Engineering Association (PCEA). To read past columns or contact Dack, click here.

Transforming Electronic Systems Design

Article by David Wiens
SIEMENS DIGITAL INDUSTRIES SOFTWARE

The electronics industry is entering a new era of digital transformation driven by the urgent need for electronic systems companies to overcome three big design challenges—product, organizational, and process complexity.

These three challenges are looming larger than ever as companies work to create modern-day, even futuristic, products that weld electrical, mechanical, and software design together, and they have to do so under the strain of shrinking design and production schedules and an unprecedented pace of innovation.

Companies can no longer afford the old way of doing things, such as building multiple prototypes and running them through several test iterations. Indeed, the classic prototyping-dependent approach actually contributes to missed schedules, increased development expenses, and degraded product quality.

The negative impacts of not adopting new ways of doing business are significant. Recent research by LifeCycle Insights shows that 58% of all new product design projects incur unexpected and unbudgeted additional costs and time delays. Only one in four projects actually goes out on time and on budget. To meet schedules, engineering teams often cushion 3–4 respins into their cost and time estimates, thus perpetuating process inefficiencies.

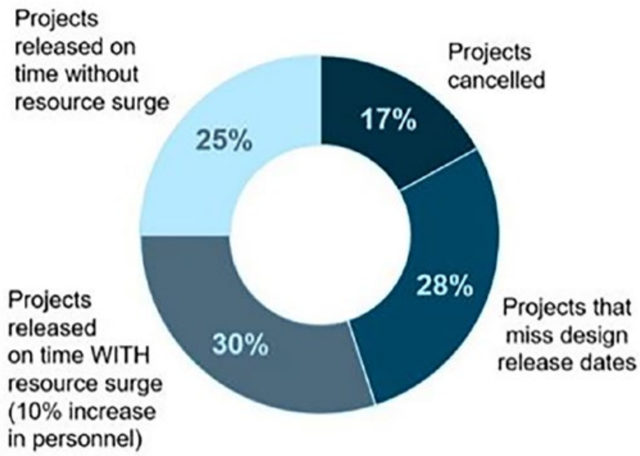


Figure 1: A total of 58% of all projects incur additional costs or miss release dates. (Source: LifeCycle Insights)

The Big Three Complexities

Product complexity has grown significantly with the advent of advanced node ICs, faster DDR memory, and SerDes buses. For example,

Figure 2: Product, organizational, and process complexity lead to increased costs, lower design quality, and missed schedules.

running signal and power integrity analysis on multi-board designs can be very tricky, and multi-board systems come with difficult connectivity requirements between boards and between boards and mechanical enclosures. Even simpler designs that use the latest generation FPGAs and DDR memory require signal and power integrity analysis.

All of this comes at a time of extreme schedule pressure, where the expectation is to get it right the first time, so engineering teams have to get the analysis done quickly and done right. The drive to reduce electronic form factors also drives product complexity, with tighter tolerances between PCBs and enclosures and advanced manufacturing technologies like rigid-flex, HDI, and embedded components.

Organizational complexity becomes more entangled as large teams specialize, and distributed groups are leveraged to develop a single product. These different design teams often operate independently or in isolation and have poorly defined touchpoints. Using design tools that cannot share data seamlessly between disciplines often leads to problems found very late in the design cycle or after physical prototypes are built.

Product and organizational complexities also complicate the core processes throughout the entire development flow—from product concept to architectural decomposition, all the multiple parallel domains for electronics, mechanical, software, and finally, manufacturing. Not only do designs need to meet all their functional requirements, but the software that interfaces with the hardware must also work properly. Additionally, all products must meet strict guidelines for their intended operating environments as well as for manufacturability and, in a number of industries, products have to meet a set of complicated regulatory standards.

Succeeding With Complexity

Overcoming these complexities demands a digital transformation strategy that addresses inefficiencies and optimizes both electronic and multi-domain systems design and verification. By embarking on this digital transformation, companies will break down the barriers between teams, eliminate physical prototypes, and manage IP across the enterprise.

A successful next-generation design platform must support integration, shared data, and improved intelligence. Integration across design processes and disciplines optimizes resources to reduce development time and cost. Sharing context-specific design data reduces design cycles and costs due to fewer data fidelity-driven respins. Improved intelligence provides actionable information and feedback loops to inform cost and resource management decision-making through metrics-driven prescriptive analytics.

In turn, to deliver these three keys to product differentiation, profitability, and beating the competition to market requires five transformation capabilities.

Digitally Integrated and Optimized Multi-Domain Design

Digitally integrated, optimized multi-domain design establishes a digitally integrated solution across multiple domains to reduce manual intervention, foster collaboration, and improve transparency across disciplines. In creating a digital thread between domains, they establish traceability and interactivity from one domain to the other. This digitally integrated environment enables efficient, secure, concurrent design across all engineering teams, whether individual contributors work at the same site or across the world.

A digital thread between design and manufacturing enables teams to minimize the respins that often happen between the design and manufacturing teams. Integration between design and manufacturing is essential for producing products that are high quality, low cost, and on time. A digitally integrated solution enables teams to optimize the costs associated with a project, accelerate design time, manage data integrity, and improve the quality of results.

Model-Based Systems Engineering (MBSE)

A model-based systems engineering approach from product requirements through manufacturing helps engineering teams solve the multitude of complex and challenging tasks presented by full system design. It allows team members to view the entire system and model pieces of that system individually, earlier in the design flow. It does not matter if those pieces are on the electronics side, the electrical side, the mechanical side, or the software side.

By looking at the entire system through a model-based systems perspective, teams can not only look at the electrical and functional trade-offs earlier in the design cycle, but also product trade-offs that might be based on such things as weight, cost, or even available components. And by leveraging the techniques of MBSE, interfaces can be established very early in the design cycle between each of the individual domains. In doing so, the implementation within each domain can be isolated from the others. This allows engineering teams to work in parallel, and it gives an earlier view of the entire product that the team seeks to develop.

Digital Prototype-Driven Verification

By integrating verification throughout the multi-board electronics design process—starting very early, long before physical prototypes—engineering teams can smooth the entire design process and increase design quality through digital-prototype-driven, shift-left verification and cross-domain modeling. Shifting verification to the left in the design flow using automated, integrated tools reduces product schedules and increases the likelihood of on-time product launches. Cost and time are saved by finding problems early during design, minimizing design iterations, and manufacturing respins.

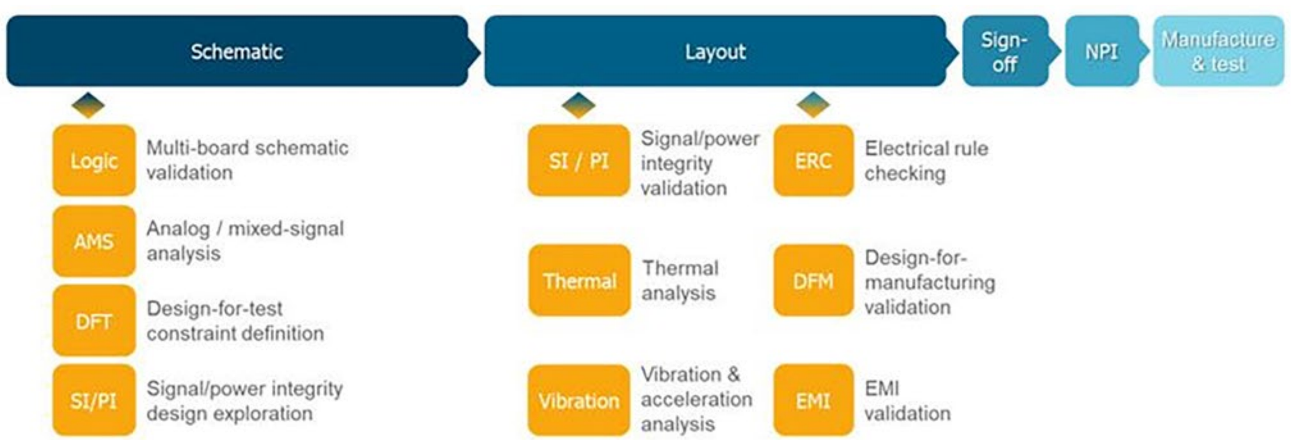


Figure 3: Teams can catch more errors earlier by integrating verification throughout the design process.

Because a shift-left verification strategy provides efficient, early detection of failures, it is possible to evaluate functional, electrical, thermal, and manufacturability trade-offs when they are easier and cheaper to modify, fix, and compare. It also supports cross-domain digital modeling and simulation without waiting for physical prototypes. Instead, digital prototypes drive verification. Given this ability to evaluate alternatives, the cost of the overall system can be greatly reduced.

Capacity, Performance, Productivity, and Efficiency

Process automation, abstraction, reuse, and scalable tool capacity sustain engineering productivity and process efficiency regardless of design complexity, so design and process complexity won't bog everything down. A next-generation systems design platform must provide scalability so it can be tailored to the user's needs based on their organization's size, challenges, and design team expertise.

The platform must be able to predictably and reliably manage complex designs with, for example, a very high number of pins, nets, rules, and constraints, and it must deliver interactive and automated performance irrespective of design size, complexity, or capacity. Automation of several key steps throughout the process—from schematic to layout and even verification—enables designers to be more productive while ensuring they are still in control of the design.

Supplier Strength and Credibility

To facilitate the successful adoption of a digital transformation strategy, companies need EDA tools backed by a global supplier that can develop, enhance, and support next-generation design platforms. When selecting a next-generation systems design platform, the natural tendency may be to focus on the solution and the technology behind it. And those are important.

But companies should also look at the credentials of the software tool supplier. Are they only a supplier, or are they capable of being a business partner that can contribute to your company's success? **DESIGN007**

David Wiens is a product marketing manager with Siemens Digital Industries Software.

Vishay Aluminum Capacitors Increase Design Flexibility, Save Board Space

Vishay Intertechnology has launched a new series of low-impedance, Automotive Grade miniature aluminum electrolytic capacitors that combine high ripple currents up to 3.36 A with high temperature operation to +125 °C and very long useful life of 6,000 hours at 125°C.

Compared to previous-generation solutions, Vishay BCcomponents 190 RTL series capacitors offer lower impedance and 10% to 15% higher ripple current. This allows designers to utilize fewer components, increasing design flexibility and saving board space. In addition, the AEC-Q200 qualified devices are available in smaller case sizes, ranging from 10 mm by 12 mm up to 18 mm by 35 mm.

Featuring radial leads and a cylindrical aluminum case with pressure relief, insulated with a blue sleeve, the 190 RTL series offers rated voltages up to 50 V, capacitance from 100°F to 6800°F, and low maximum impedance down to 0.017 Ω. The capacitors are charge- and discharge-proof.

As polarized aluminum electrolytic capacitors with a non-solid electrolyte, the RoHS-compliant devices are ideally suited for smoothing, filtering, and buffering in switch mode power supplies and DC/DC converters for high temperature industrial, automotive, telecommunications, medical, and military applications.

(Source: Globe Newswire)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Simulation Slashes Iterations

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

The majority of high-speed digital designs take at least two iterations to develop into a working product. However, these days, the product life cycle is very short; therefore, time to market is of the essence. An aggressive timeline can mean that a re-spin is not possible. Plus, it will cost more than just engineering time; one must also consider the cost of delaying the product's market launch. This missed opportunity could cost hundreds of thousands of dollars.

However, multilayer boards can be designed to work right the first time with little additional effort, providing you follow a tried and proven process that results in a reliable, manufacturable design that performs to specifications and is produced on time and to budget. One of the most frustrating aspects of PCB design is when you have to redo work that has already been completed. Yet design re-spins will continue to happen until designers make regular use of simulation software.

Complex multilayer boards should be designed using a proven design methodology, incorporating pre-layout simulation before placing a single chip on the board. Simulation tools can be used to analyze various signal integrity (SI) issues like reflections (due to impedance mismatches), crosstalk, signal attenuation, stackup and power distribution network (PDN) impedance, and noise—all of which can impact interconnect performance.

Unfortunately, simulation is often engaged toward the end of the design cycle, which is too late. Ideally, the simulation should be done during the design process as part of standard practice. The post-layout simulation should be the final PCB design process, not the first. If changes are made late in the design

process, then it takes more time, people, material, and money.

This is where board-level simulation cuts re-spins: A pre-layout simulation identifies issues in the conceptual stage so that they can easily be avoided, and the post-layout simulation catches the issues during the design process eliminating the potentially disastrous final stage changes. Of course, you also need to keep your eye on the ball during the entire design process, catching any small issue before it becomes a major problem. This is the most cost-effective way to design a board with fewer iterations rather than starting with the "find-and-fix" post-layout simulation approach.

There are multiple facets to board-level analysis, including:

- Stackup planning for controlled impedance, SI, crosstalk, and cost control
- Dielectric material selection for manufacturing yield and high-frequency operation
- Transmission line termination strategy
- Floor-planning for critical components
- Deriving layout routing constraints, including trace width, spacing, and delay matching
- PDN optimization
- I/O buffer and drive strength selection
- Topology optimization
- SI analysis to meet the design specifications, with respect to noise margins, timing, skew, crosstalk, and signal distortion
- Estimated electromagnetic radiation

The board stackup configuration is the most often overlooked issue in the early design stages. The majority of designers leave the stackup planning to deal with at design completion, along with fabrication deliverables. Before starting a PCB design, you need to plan the PCB stackup and impedance to ensure that the selected substrate materials are available from your chosen fabricator—a step that is regularly missed. Changing the stackup toward the end of the design process could mean changing trace widths and clearances to achieve the correct impedance, which could create a lot of unnecessary work.

If you use the same materials that the fab shop stocks to build your stackup, then the impedance will be more accurate (Figure 1). If we just choose a convenient (virtual) number for core thickness, for example, then this may

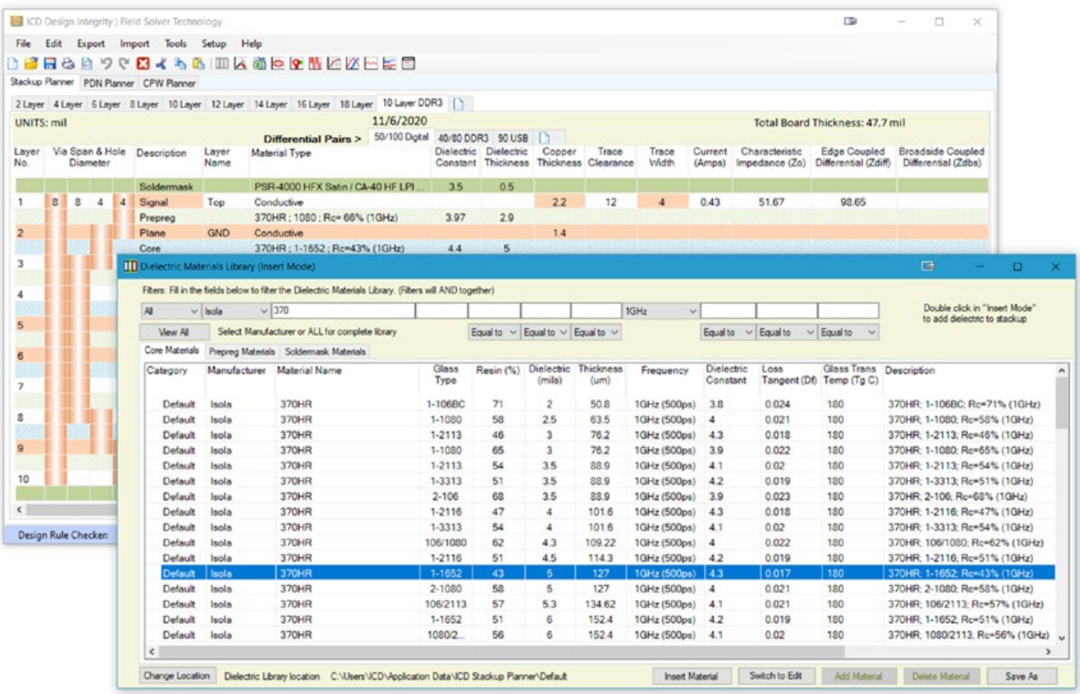

Figure 1: The dielectric materials library lists the fabricator's stocked materials (iCD Stackup Planner).

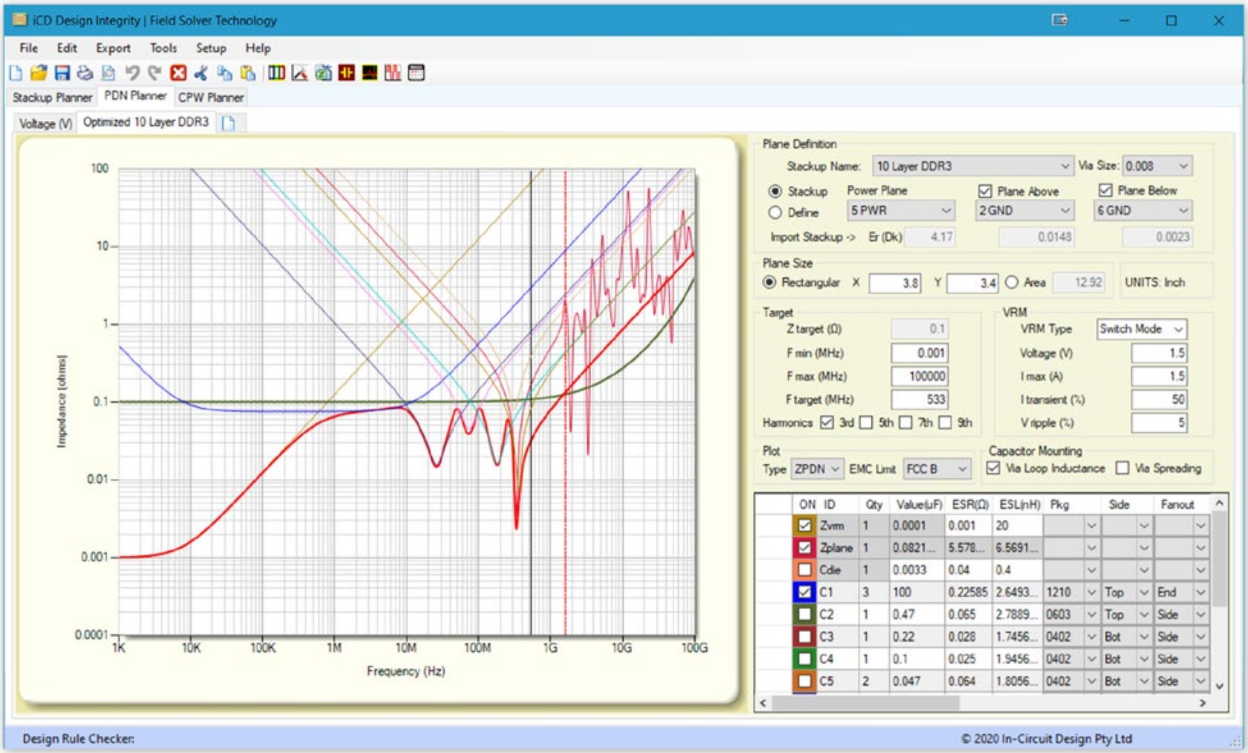

Figure 2: Optimized DDR3 PDN (iCD PDN Planner).

be up to 3% different from what is available; hence, the impedance will vary by 3%. Incorrect impedance creates reflections that lead to downstream SI, crosstalk, and radiation issues.

The design of the PDN is also a very important part of the conceptual design process, ensuring that you have a stable power delivery system before you even start placing a chip on the board.

Decoupling and bypass capacitors supply instantaneous current at different frequencies to the drivers until the power supply can respond. In other words, it takes a finite time for the current to flow from the power supply circuit (whether on-board or remote) due to the inductance of the trace and/or leads to the drivers. Decoupling capacitors also lower the impedance at different frequencies to help meet the AC impedance target.

Every decoupling capacitor has an equivalent series inductance (ESL) and mounting inductance that causes its impedance to increase at high frequencies. To reduce this inductance as much as possible, several small value decaps should be spread throughout the PDN. These decaps interact to create anti-resonance peaks but should work together to lower the AC impedance. This is a trial-and-error process and needs to be done with the assistance of a PDN analysis tool (Figure 2).

A post-layout simulation requires the translation of the design files so that they can be read into the simulator. The simulation software should interface to all major EDA PCB design packages. However, if you have a simulation tool that is built into the PCB design software, then critical signals can be readily simulated by extracting the topology into the simulation environment. This creates a free-form schematic of the transmission lines, including drivers, microstrip and stripline modules, vias, and loads.

A batch mode simulation identifies possible SI, crosstalk, and EMC violations. Interactive simulation is then used to further analyze these potential issues. Crosstalk is typically picked up on long parallel trace segments. These can be on the same layer, as in Figure 3, but may also be broadside coupled from the adjacent signal layer. It is for this reason that orthogonal routing is recommended on adjacent signal layers (between planes) to minimize the coupling area.

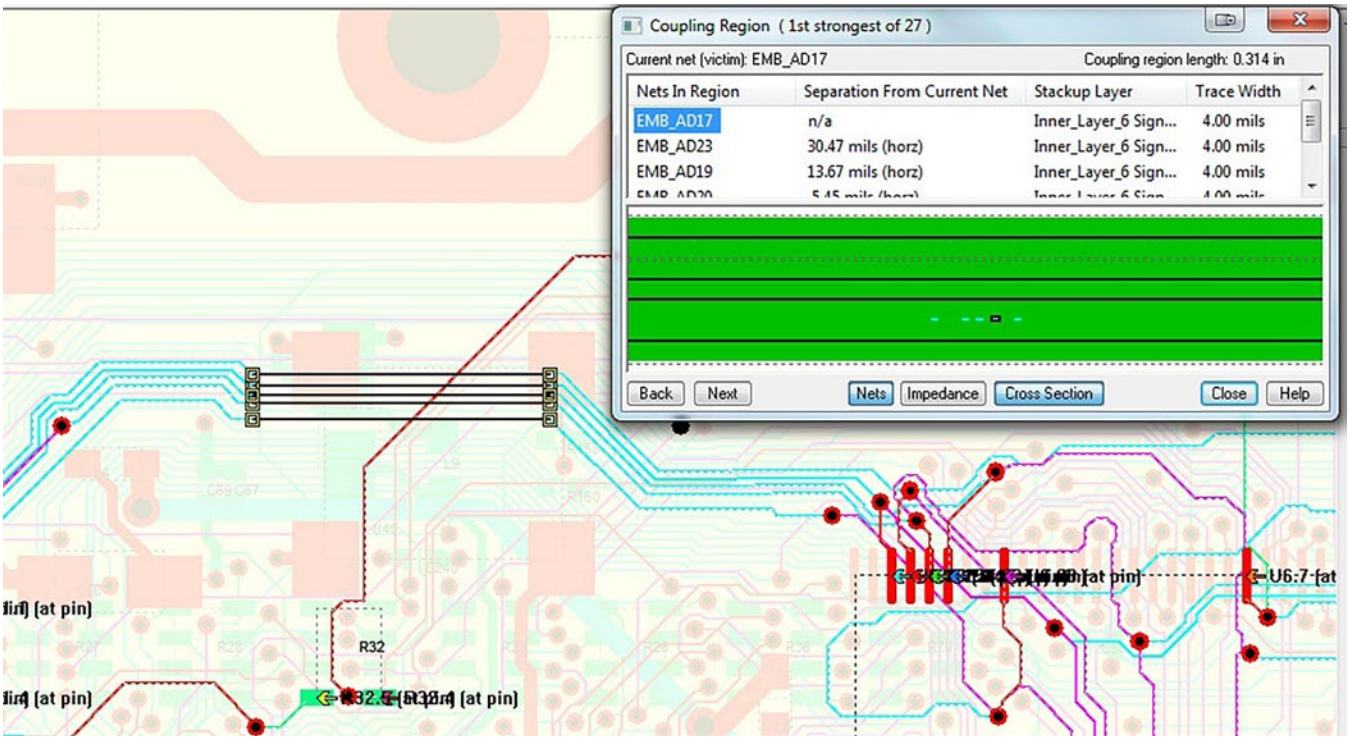

Figure 3: Crosstalk on long, parallel trace segments.

Flight times of the critical signals should be examined. One could compare the matched lengths of each signal, but the delay will vary depending on the meander pattern and stackup layer. Thus, it is important to match delays, not lengths (Figure 4).

Since all products must comply with strict electromagnetic compliance (EMC) regulations, all critical signals should be simulated to determine the amount of expected radiation. Don't let your project call for Plan B, which is basically disaster recovery.

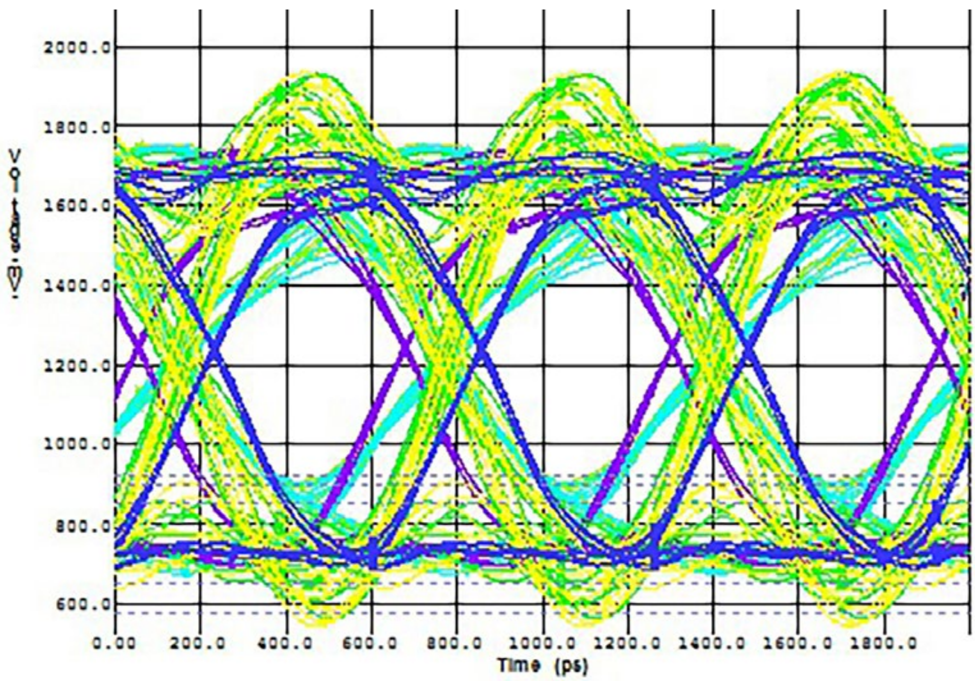

Figure 4: Skew of the clock to address, control, and command signals.

If, for instance, on the third iteration, your product still does not meet specifications, and management is pushing to have the project completed, then you may need to look for new employment opportunities. However, if simulation is done during the design process, then these re-spins can be avoided, keeping your project on budget and on schedule.

Key Points

- The product life cycle is very short; therefore, time to market is of the essence
- Multilayer boards can be designed to work right the first time with little additional effort, providing you follow a tried and proven process
- Re-spins will continue to happen until designers make regular use of circuit simulation software
- Simulation is often engaged toward the end of the design cycle, which is too late
- Ideally, the simulation should be done during the design process as part of standard practice
- A pre-layout simulation identifies issues in the conceptual stage
- The post-layout simulation catches the issues during the design process, eliminating the potentially disastrous final stage changes
- Keep your eye on the ball during the entire design process, catching any small issue before it becomes a major problem
- Before starting a PCB design, you need to plan the PCB stackup and ensure that the selected substrate materials are available from your chosen fabricator
- If you use the same materials that the fab shop stocks to build your stackup, then the impedance will be more accurate
- The design of the PDN is also a very important part of the conceptual design process, ensuring that you have a stable power delivery system
- Decoupling and bypass capacitors supply instantaneous current at different frequencies to the drivers until the power supply can respond
- Decoupling capacitors also lower the impedance at different frequencies to help meet the AC impedance target
- PDN design is a trial-and-error process and needs to be done with the assistance of a PDN analysis tool
- If you have a simulation tool that is built into the PCB design software, then critical signals can be readily simulated by extracting the topology into the simulation environment
- Crosstalk is typically picked up on long parallel trace segments on the same layer but may also be broadside coupled from the adjacent layer
- One could compare the matched lengths of each signal, but the delay will vary depending on the meander pattern and stackup layer. Thus, it is important to match delays, not lengths **DESIGN007**

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- B. Olney, "Beyond Design: Board-Level Simulation and the Design Process: Plan B–Post-Layout Simulation," *The PCB Magazine*, February 2012.
- B. Olney, "Board-Level Simulation," *Electronics News*, Australia, February 2013.

Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at icd.com.au. To read past columns or contact Olney, click here.

Is 2020 Really Coming to an End?

Connect the Dots

by Matt Stevenson, SUNSTONE CIRCUITS

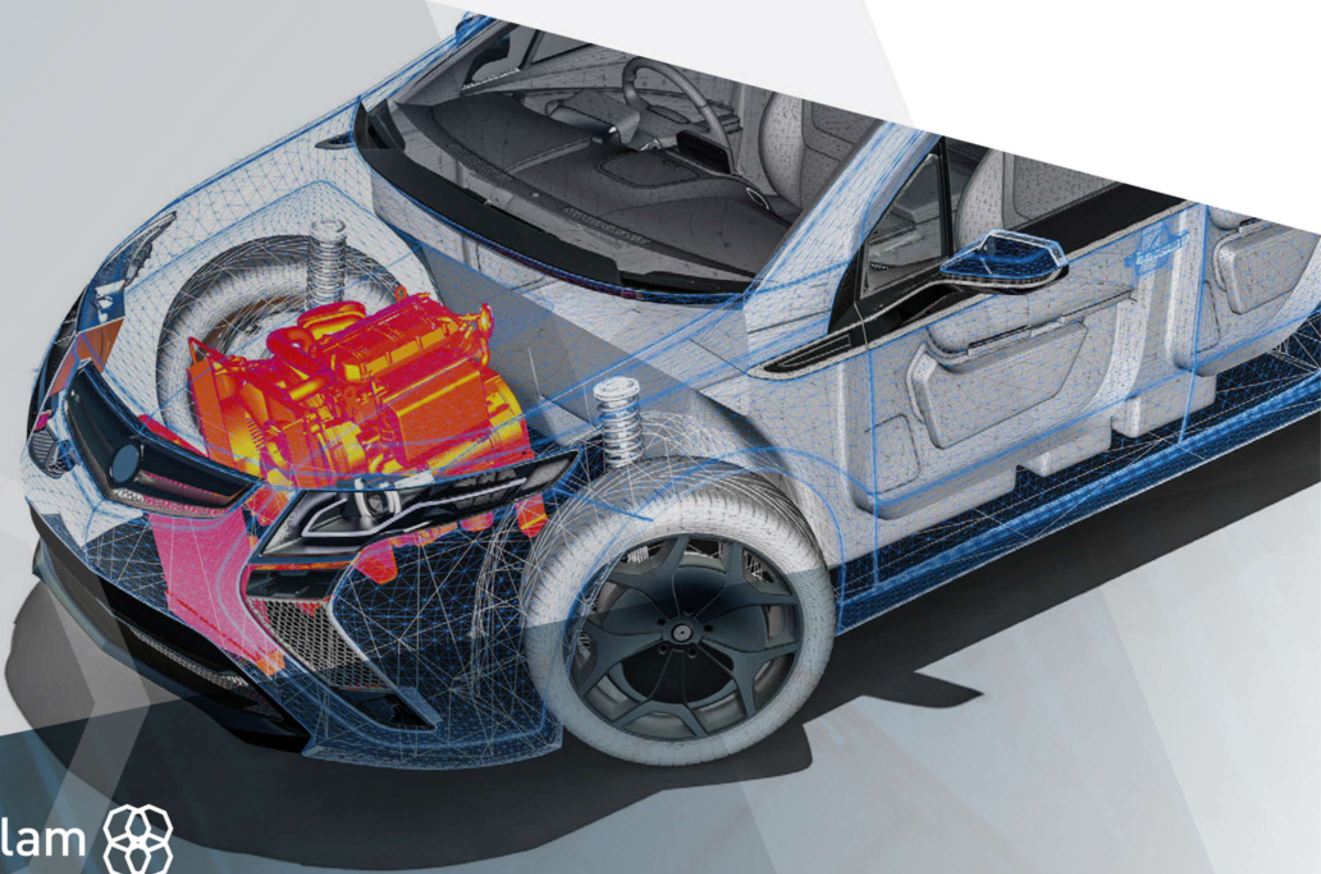
As we approach the end of 2020, we are able to look back on one of the most challenging years that I have ever experienced. But it is not just me; this year has been one to remember (not really fondly) for everyone on the globe. We are very fortunate to have been able to carry on with supplying PCBs to a great number of people and industries, even in the midst of our COVID-19 pandemic. We were also fortunate to be a key supplier for multiple projects aimed directly at helping with the pandemic.

Throughout these trying times, we have been consistent in our desire to share knowledge with everyone and give ourselves and everyone else a few minutes' break from our reality. The following is a synopsis of the topics we shared with you from the perspective of a PCB manufacturer.

1. January (Design Tips for Layout): Here, we share tips as a manufacturer that has seen thousands of PCB layouts. Some examples are very good, but we also describe pitfalls to avoid that might give you a chuckle or two.

2. February (You Cannot Afford Not to Consider ISO:9001): The International Organization for Standardization (ISO) 9000 family and ISO 9001 certifications are built on standards achieved with a QMS that addresses far more than "just quality." Done correctly, we learned that this standard provides a foundation for a robust business management system. It was a journey worth taking, and one we encourage you to consider. Fair warning: ISO adoption can be challenging at times.

3. March (The Seven Year Etch): Creating the copper circuitry on a PCB involves etching. The more that is known about how a PCB is made, the better equipped a designer will be to create the design.



4. April (Increased Focus on Health and Wellness Transforms the PCB Industry): Our increased focus on health and wellness drives technology advancement for personal devices, and those used in the delivery of healthcare. This trend also drives both PCB production innovation and a long-overdue update of the employer/employee relationship.

5. May (Picking a Phototyping Strategy): Since no two design projects are the same, your approach to prototyping should be flexible. Your needs will be different every time. Are you going for fast-and-dirty prototyping? Do you need a quick turnaround time? Will it be easier for you to use a DIY prototyping technique?

6. June (The Power of Forward Thinking): Innovating is fun, and creativity can be a good outlet for people, but PCB design seems to be a rigid set of rules and not fun or creative. However, it really can be an opportunity to have fun and be creative and still create a highly effective and manufacturable PCB.

7. July (Reassessing the Risk of Offshore PCB Manufacturing): Making the right decision about domestic versus offshore PCB manufacturing depends on a thorough cost-benefit analysis. Your results will vary depending on volume and design requirements. We encourage our customers to look for the hidden costs in offshoring and seriously consider its less quantifiable pain points.

8. August (The Nuts and Bolts of Electrical Testing): Understanding the process of electrically testing a bare PCB is key. The more that a designer can understand the manufacturing and testing processes, the better the PCB design. This column imparts some of the key points around electrical testing.

9. September (How to Know If a CAD Tool Is Right for You): The most important tool that a PCB designer can have at their disposal is the CAD tool. There are many different tools available, ranging from very simple and free to super powerful and expensive and everything in between. Depending on the goal of a particular project, many designers have several in their tool belt. This column explores what to look for in a CAD tool. It can be a very personal choice, but knowing what to look for can make that search more productive.

10. October (Unraveling the Mysterious BGA Routing Mess): In an effort to pass on many tips to help become a better PCB designer, this column was aimed at solutions to make the process of routing a sometimes tricky BGA component easier using logical steps to make it happen. Sometimes, left to their own processes, the resulting design may not be a treat to manufacture. (The more you know.)

11. November (The New Recipe for Customer Service Success): What does customer service look like now in the midst of the pandemic? What does it need to look like to meet and exceed the needs of the customer? Al Secchi, global customer support and sales manager, shares his thoughts.

Bob and I had a lot of fun sharing some of what we have learned in our over 60 years of combined PCB experience. With that much time in the industry, there are so many tips, pitfalls, stories, and knowledge tidbits that we can still share. We are really looking forward to a year of growth and higher expectations as more and more people get back to work, adapt to this new normal, and continue to innovate, create, and design. If there are topics that you are interested in us exploring, reach out to us and let us know what is on your mind. **DESIGN007**

Matt Stevenson is the VP of sales and marketing at Sunstone Circuits. To read past columns or contact Stevenson, click here.

PCB007 Highlights

PCB Technologies Focuses on an All-in-One Solution ▶

Recently, PCB Technologies reached out to us with news about their new All-In-One offering. Intrigued, we followed up and spoke with VP of Marketing and Business Development Arik Einhorn to get more details on the All-In-One services. We've included the short article and the interview below.

Manufacturers Weigh in on Made-in-America Debate ▶

As the U.S. grapples with who will take the helm of the U.S. presidency, electronics manufacturers around the country are grappling with which policies and ideas would promote growth and innovation in the sector. Many agree that a push for "made in America" policies and incentives might be useful. Often, they point to similar initiatives used by other countries, including China and India.

Gardien on the Right Track With New ERP System ▶

Andy Shaughnessy speaks with Roland Valentini, Gardien Group COO, about the company's new OnTrack2 ERP and process management software. He explains how OnTrack2 is purpose-built for customers around the world and why it's much more than a replacement for OnTrack1, which was being stretched beyond its original intent.

TTM Technologies: Defense, Data Drive Profits in 3Q ▶

TTM Technologies Inc., a global printed circuit board (PCB) and radio frequency (RF) components manufacturer, reported results for the third quarter of fiscal 2020, which ended on September 28, 2020.

Survey Results: 'Are You Currently Hiring?' ▶

The I-Connect007 research team invited readers to share their thoughts on what's happening with staffing and retention to help prepare for an upcoming issue on this important topic. Here, we delve into the first question, "Are you currently hiring?"

EPTE Newsletter: Recent Market Trends in Japanese PCBs ▶

The Ministry of Economy, Trade, and Industry (METI) released the August production data from Japan. Dominique Numakura explains how they did during the COVID-19 pandemic.

The PCB Norsemen: So Much More Than Just Through Vias ▶

As most people know, component holes are still highly necessary for components that require them, and clean lead-through-holes (vias) have increased in necessity over the last 30 years. John Steinar Johnsen explains how the challenges with smaller diameter vias, perhaps depth-controlled, have increased and are, in some cases, challenging for those who produce PCBs and have to assemble and handle solder components.

HKPCA's Audrey Sim Details Upcoming Electronic Circuits World Convention ▶

Nolan Johnson speaks with Audrey Sim, executive director and vice president of operations for the Hong Kong Printed Circuit Association, about the upcoming Electronic Circuits World Convention, to be held November 30 through December 2, 2020. Ms. Sim gives Nolan an overview of the conference's history, its scope as a printed circuit industry conference, and its shift to a hybrid virtual/physical format for 2020.

Understanding Material Interactions With PCB Fab Processes

Lightning Speed Laminates

by John Coonrod, ROGERS CORPORATION

Having a good understanding of the circuit material that a designer is working with, along with the potential PCB fabrication influences, is essential for having a successful first-time evaluation of a new circuit design. If a designer only considers the basic material properties of Dk and Df, that may not be enough information to have a successful first round of evaluations.

The Dk and Df values that are found on a material datasheet are typically generated with a non-circuit test method, which is usually a raw material test that is using some type of fixturing. If that same material is evaluated in circuit form, it is very common that the Dk and Df values will be different because the propagating wave on the circuit may have different influences than in a test fixture. Understanding how a circuit material behaves in circuit form can be very valuable to the circuit design process for achieving better circuit performance for the evaluations of a new design.

A topic that has been getting more attention over the past several years is copper surface roughness. The copper surface of concern is at the substrate-copper interface as a laminate is made and not the air side of the laminate. However, depending on how the circuit is made, the copper surface on the air side of the laminate can play a role in the impact that the surface roughness has on circuit performance. The copper surface roughness effect has been found to influence insertion loss, phase response, and propagation speed.

In a very general sense, when the speed of an electromagnetic wave is analyzed, a slower velocity will indicate a higher Dk value of the wave propagation medium. If two similar circuits are evaluated for the extraction of the material's Dk value, the circuit with the slower

wave speed (or increased propagation delay) will report a higher Dk value.

There are other circuit and material properties which can slow the propagating wave, besides the Dk of the material. The copper surface roughness can slow the wave and cause the Dk extraction from the circuit evaluation to report a higher Dk than what the material possesses. We conducted a simple experiment years ago that conclusively showed the influence of copper surface roughness on the Dk extraction process. Figure 1 provides a simple overview.

Figure 1 shows the results of testing laminates in circuit form, using the microstrip differential phase length method, which uses microstrip transmission line circuits of different lengths. Before the laminates were made, the copper surface roughness was evaluated using a non-contact laser profilometer, and the average roughness values are reported in the legend of the chart.

After determining the surface roughness of these four different types of copper, the same dielectric material was used to make four laminates. The laminates were fabricated into microstrip circuits and evaluated for effective dielectric constant based on phase angle measurements. The effective dielectric constant (the Y-axis of Figure 1) is the dielectric constant that the wave experiences. For a microstrip circuit, it is a combination of the dielectric constant of the substrate and air.

Figure 1 shows four distinct trends of an increased Dk curve for an increased copper surface roughness. Basically, circuits using a smooth copper (red curve) will not slow the wave much, and the reported effective Dk will be closer to the ideal value. A circuit using copper with a much rougher surface (blue curve) will slow the wave significantly, and the reported effective Dk value will be much higher than the ideal effective Dk value of the substrate-air combination.

Keep in mind that the same dielectric material was used for collecting data reported in this chart, and there is a difference of 0.3 for effective Dk, which is due to differences in copper surface roughness only. This is very important because if the dielectric material is evaluated in a fixture without copper roughness effects, the Dk values will be significantly different than shown in this chart. Additionally, if a thicker substrate is used, which implies the copper planes are farther apart, the influence of copper surface roughness is reduced, and the reported effective Dk value will decrease. The copper roughness effects can be very important

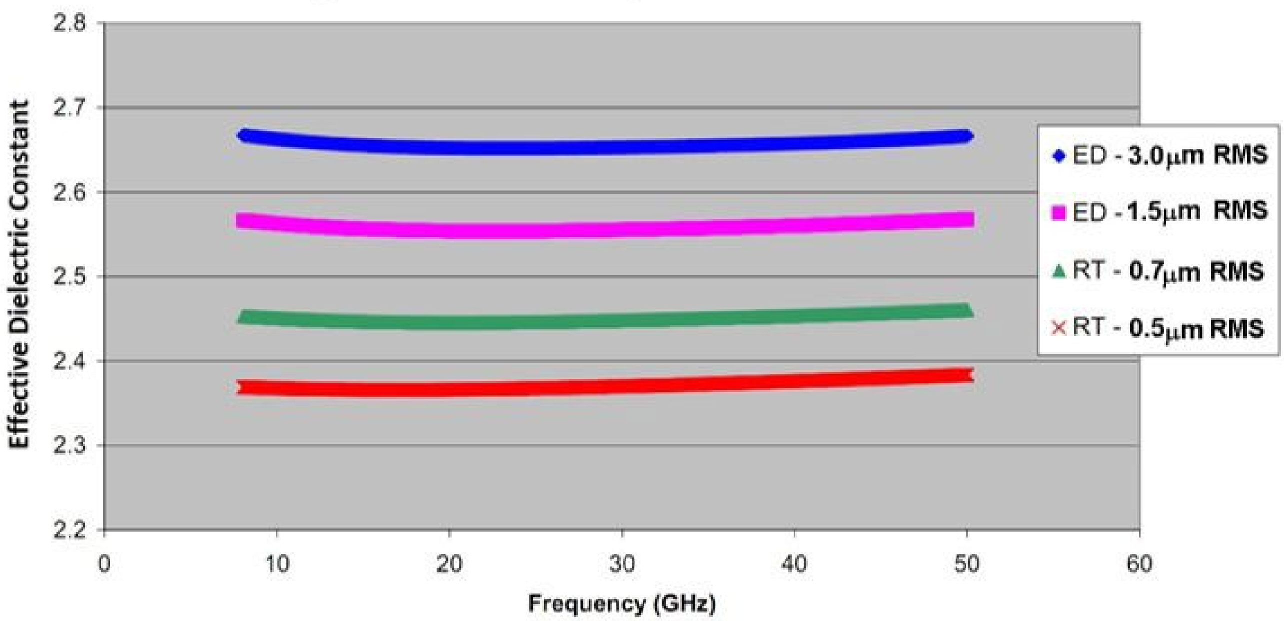


Figure 1: A 4-mil LCP laminate effective dielectric constant vs. frequency for various copper foil types on a 50-ohm microstrip transmission line.

to understand for determining the proper Dk value to use for circuit design and simulation.

There is a complication in which the circuit design and construction can be more or less sensitive to the copper surface roughness effects. The microstrip circuit example given is relatively easy to understand for the effects of copper surface roughness. However, for a stripline circuit, which has four substrate-copper interfaces, the influence of surface roughness on circuit performance is more complicated. The stripline circuit can have very different surface roughness effects due to how the circuit is constructed. A stripline circuit fabricated using a foil lam construction can have a very different copper roughness influence than a stripline made as a core lam construction.

There is also the potential influence of some PCB fabrication processing effects on the extracted Dk of a material when tested in circuit form. One of these influences can be the copper plating thickness and its normal variation. Another influence can be the final plated finish and its variation. The copper plated thickness and its variation, as well as the final plated finish and its variation, can have a significant impact on circuit features that are edge coupled.

These potential influences on circuit performance, which can affect the extracted Dk value of the material, will depend a lot on the circuit design and construction. Most designers consider the final plated finish in relation to insertion loss differences; however, the plated finish can certainly impact the phase response of the circuit, which can alter the extracted Dk value of the material from a circuit evaluation.

The bottom line for getting good results for a first-time evaluation of a new circuit design is for the designer to understand the material properties, test methods, and influences of circuit fabrication for their particular design concept. These are a lot of issues to consider, and it is best to have the designer work closely with their material supplier and the PCB fabricator to ensure the best results for the initial circuit evaluation of a new design. **DESIGN007**

John Coonrod is technical marketing manager at Rogers Corporation. To read past columns or contact Coonrod, click here.

Figure It Out: Field-Programmable Battery Array (Unsolved)

by Dugan Karnazes
VELOCITY RESEARCH

I went into the field of engineering to solve problems and come up with practical solutions. But every now and then, a solution comes up that is today unbuildable.

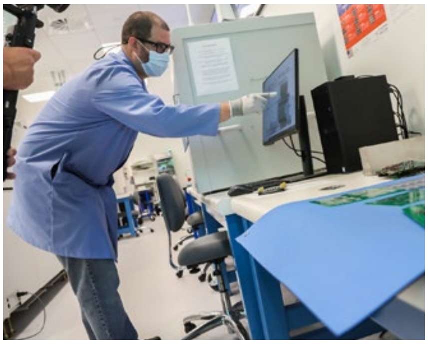
I would like to introduce you to a problem that has been bouncing around in my head: the field-programmable battery array.

One of the notable design challenges with this is the limitations of today's transistors. I fully acknowledge that this design is impractical today, but with better transistors (or a better designer), that could change. As history shows us, anyone who has bet against the advancement of transistors has been disappointed, so I hold hope that one day, this idea will be practical. This is more of a thought experiment, but perhaps one of you can get further with it than I have.

To read the full column, click here.

Dugan Karnazes is the founder and CEO of Velocity Research.



Lorain County Community College's Successful MEMS Program

Interview by Andy Shaughnessy
I-CONNECT007

In a recent conversation with Johnny Vanderford, assistant professor and coordinator of Lorain County Community College's microelectromechanical manufacturing systems (MEMS) program, we discussed the school's model for a successful technical higher-education program and what students learn about PCB design. Vanderford is also the director of the new Manufacturing Electronics and Rework Institute for Training (MERIT) coming to the college.

Andy Shaughnessy: Johnny, I see that you teach design. It looks like it's tied in with manufacturing, and that's a good thing. We hear stories about EEs graduating and going to work in a company, and they say they have PCB experience, but they don't know what copper pour is. In this program, what do they learn as far as design goes?

Johnny Vanderford: In the first year of the program, they begin the first week by soldering surface-mount components to PCBs. We start talking about terminology on the boards, pads, vias, silkscreen, and laminate. Also, in the first part of the degree, in addition to taking your run-of-the-mill electronics classes, they take courses in AutoCAD drafting, as well as SolidWorks. They learn some basic drafting programs.

In the second year of the program, they fabricate PCBs by applying plots on top of boards that have photoresist on them. We show them that the plot is artwork. This is mechanically-drawn artwork that has been drawn up in CAD and that shows them how to basically fabricate their own board on just a single copper layer.

In the following semester of the second year, they learn how to design their first board using an online PCB design program. Currently, we use EasyEDA and have incorporated using it as a mechanism for teaching the basics of PCB design. For instance, they learn how to draw up the schematics, what nets and library files are, how to create a bill of materials (BOM), and how to draw up the layout so that their board can be laid out. Primarily, it's a surface-mount board that often contains at least one sensor

Johnny Vanderford

that has a somewhat basic primitive function.

For instance, one of our last boards we made last year used a MEMS microphone and three LEDs. The louder that you talked into the microphone, the more the LEDs lit up in series. It's not a fancy PCB, but in the second year of the program, this is something where we not only teach schematics, BOM, and layout, but they also learn how to do stencil printing, pick-and-place, and reflow for that same board. It's a capstone class that's meant to give them experience using electronics, drafting, design, and manufacturing altogether.

In the third year of the program, we teach a full class in Altium Designer that shows them how to design for manufacturing. Several companies hire our students to do library file generation, so they generate library files and do some PCB manufacturing. But most of the time, they just get hired as a junior draftsperson. In addition to doing Altium to do schematics, schematic library files, BOM, layout, and the fabrication files, a particular emphasis is made on the fabrication files—especially the pick-and-place files—that get used on our equipment in their next class where they build the PCB that we get fabricated at a local company. We send that board through our stencil printer, stencil print inspection, and pick-and-place and reflow.

It's not just designed for functionality; it's designed for manufacturing to make sure that there are fiducials for the stencil printer and that there's a second set of fiducials for AOI that's not going to be printed on so that we can easily see it. They also take blueprints classes, a SolidWorks class, and geometric dimensioning and tolerancing. We get fairly deep into the design. We want them to design something that they can have at the end of the experience. Those three years are spent the most on terms of where the design is and toward making a working PCB, with the fourth year having a heavy application of design to manufacturing by running an entire SMT line, inspection equipment, and testing equipment based on a PCB that was designed in Altium.

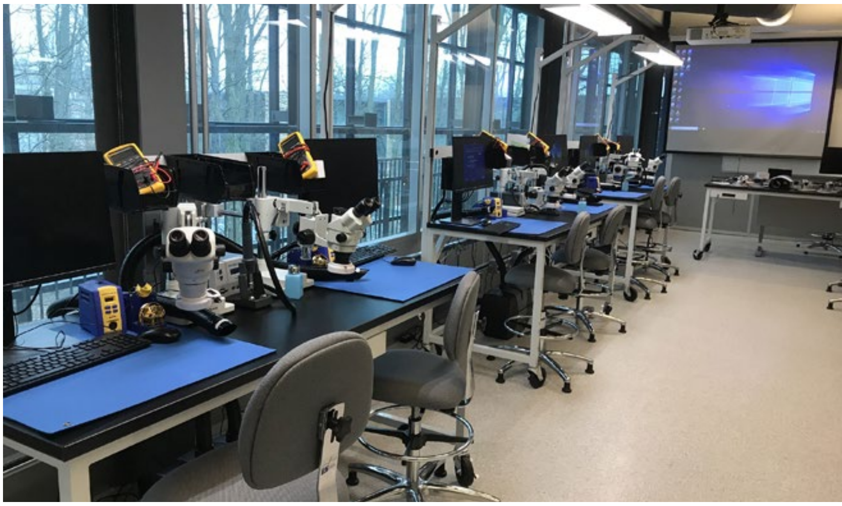
When we first made the program, I asked, "What design program is most popular?" A lot of people still use EAGLE CAD because the seat cost is cheaper, but Altium is so universally used at this point. We were considering bringing Altium into our associate's degree to eventually replace EasyEDA, but we'd have to work that in with the instructor and everything like that, so it's just one of those things. Eventually, it will come into play.

MEMS student training also includes inspection and testing.

Johnny Vanderford, assistant professor and MEMS program coordinator, demonstrates manufacturing processes in the lab.

Shaughnessy: That's good to hear. They will have some EEs coming in with some manufacturing knowledge and vice versa.

Vanderford: Right now, we're fortunate that Altium has been discounting us on our licenses. Once a year, we buy student licenses. Altium reduced the student lab fee from $100 a seat to $75 a seat, which is great. We tell the students all about AltiumLive too and say, "Look at all this" Once they see the vault of library files, they get excited.



Workbenches with inspection equipment in a MEMS program lab space.

Shaughnessy: AltiumLive has some good keynotes and talks that are available for free online, even though the event is over. Your students could watch it anytime.

Vanderford: That's cool. We love Altium. It's a fantastic program. For someone who is in the second or third year of the program, they realize it's complex. It has a lot of options, but it's one of those that we focus strongly on training. "Let's use this to design basic parts with this on here. Let's use this in relation to something that you can physically hold in your hands."

Keeping it at the community college level cost is always a challenge. For instance, we teach PCB manufacturing with SMT components, and we teach the students how to build boards. Sometimes, it's a tape and reel of some 14-pin QFP chips or something like that, and that's hard to get at a discounted price.

At the same time, we want to train them on how to program the pick-and-place so that it can pick up the parts with the correct pitch, the correct heights, and the correct tape and reel. We're very fortunate that we've had several of our advisory committee members donate expired products to us—companies like RBB, Valtronic, Vexos, and RW Beckett. These might include capacitors beyond their expiration limits in terms of their manufacturability or QFN parts from trays that can't be used anymore—any inventory that has been done for a while. We use those parts in our curriculum because they're similar to what's being used out in the industry. We have a lot of support from our advisors from that.

Lorain County Community College students have access to the MEMS lab during evening hours as well, minimizing conflicts with their current jobs.

Shaughnessy: Thanks, Johnny.

Vanderford: Thank you. DESIGN007

To read the full interview go to the December 2020 issue of *SMT007 Magazine*.

MilAero007 Highlights

The Government Circuit: As 2021 Nears, What's on IPC's Government Policy Radar?

In the United States, Election Day 2020 has come and gone, and all signs indicate that former Vice President Joe Biden is the presumptive President-elect. It's shaping up to be a busy month here at IPC, heading into a busy new year. Chris Mitchell details some of the top issues we're following this November.

Defense Speak Interpreted: Intel Is Now Making a 'SHIP'

Perhaps you recently saw that Intel was awarded a contract for a SHIP by the U.S. Department of Defense. However, this one will not float on the water since SHIP stands for state-of-the-art heterogeneous integration prototype. Denny Fritz explains.

U.S. Air Force, Lockheed Martin to Transform Airlifters Into Potent Strike Weapon Platforms

The U.S. Air Force Strategic Development Planning and Experimentation (SDPE) Office awarded Lockheed Martin a $25-million contract to support the next phase of the service's Palletized Munitions Experimentation Campaign.

Additive Electronics TechXchange: NSWC Crane and Lockheed Martin Presentations

The Additive Electronics TechXchange this year was a virtual event. Happy Holden covers two presentations, including "Very High-Density Investigation Project" by Steve Vetter of the NSWC Crane Naval Facility and "Electronics Additive Manufacturing for Defense and Space" by Kourtney Wright, Ph.D., of Lockheed Martin Advanced Technology Center.

The Aerospace and Defense Chapter of the HIR

Nolan Johnson and Andy Shaughnessy recently spoke with Jeff Demmin of Keysight Technologies, who breaks down the work his team has done on the Aerospace and Defense Chapter of the Heterogeneous Integration Roadmap (HIR).

TTM Technologies: Defense, Data Drive Profits in 3Q

TTM Technologies Inc., a global printed circuit board (PCB) and radio frequency (RF) components manufacturer, reported results for the third quarter of fiscal 2020, which ended on September 28, 2020.

BAE Systems Outlines Support Proposal to Japan's F-X Fighter Programme

BAE Systems responded to a Request for Information (RFI) from the Japanese Ministry of Defence (JMOD), proposing a package of integration support to Japan's F-X next-generation fighter development program.

Boeing, Partners Commit to Boost Canadian Economy by $61 Billion

Through five new agreements, Boeing and its Canadian aerospace partners are preparing to deliver C$61 billion and nearly 250,000 jobs to the Canadian economy.

Sikorsky Awarded Navy Contract to Build Six More CH-53K Heavy-Lift Helicopters

Sikorsky, a Lockheed Martin company, will build six additional production CH-53K King Stallion helicopters under a new contract for the U.S. Navy. The aircraft will further support the U.S. Marine Corps in its mission to conduct expeditionary heavy-lift assault transport of armored vehicles, equipment, and personnel.

Communicating Outside the Box Is Key to Flex DFM

Flex Talk

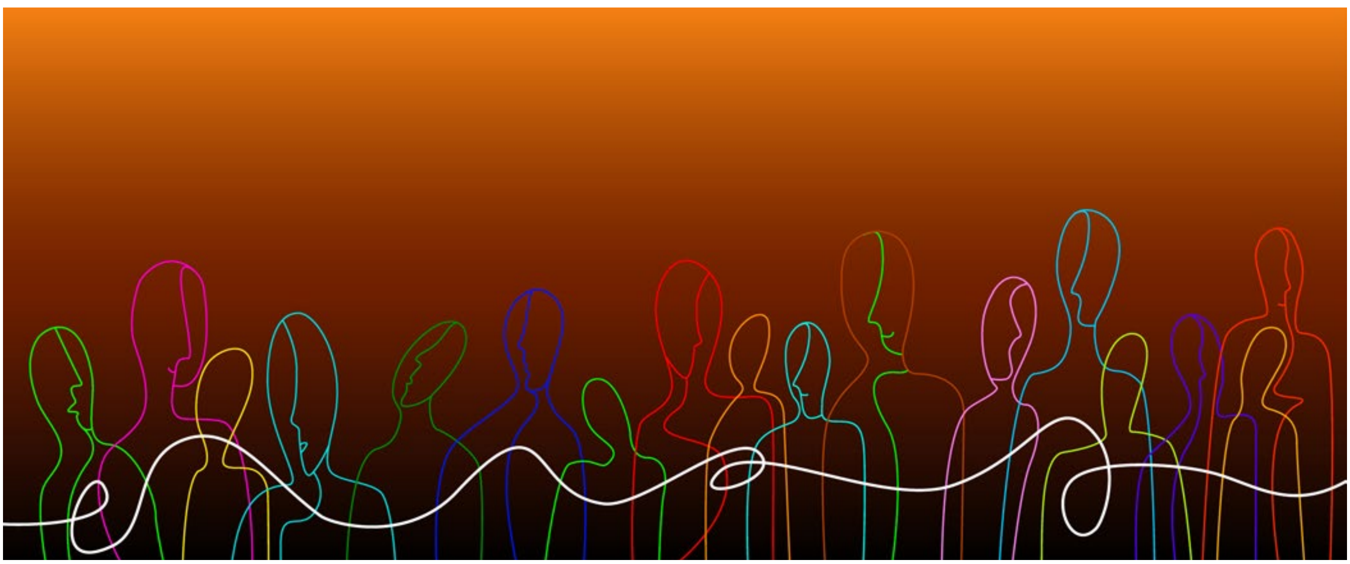
by Tara Dunn, AVERATEK

What do you do when you are designing a flexible circuit and need to go "way outside the box" to get the desired end-result? Let's look at a few success stories.

Gold Conductors

Flexible circuits are commonly fabricated on polyimide dielectrics with copper conductors. Fabricators purchase the raw material as laminate with rolled annealed copper bonded to the base dielectric. Interestingly, I have been seeing an increase in demand for gold conductors on flex materials rather than copper conductors. This combination of materials provides a much more biocompatible solution for medical applications. Exciting, right? But this significantly changes the manufacturing process and moves this design into something "out of the ordinary," which needs to be accounted for and understood in the early design phases.

To meet this requirement, the fabricator pivoted from subtractive etch processing to additive PCB fabrication technology. With subtractive etch, as the name implies, the unneeded copper is being etched away from the panel, creating the circuit pattern. While this additive technology is more commonly used for copper conductors with very fine feature sizes



THE NEXT BIG THING IS HERE

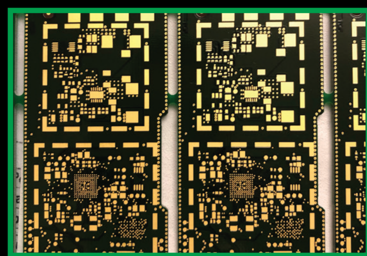
TOTAL ADDITIVE PROCESS

INKJET SOLDER MASK

SOLDER MASK

IJSR-4000 JM SERIES

- JMO2DG, JMO3G
  - Excellent Processing
  - Available in Multiple Colors
  - Available for Rigid and Flex



IJSR-4000 JM03G

LEGEND INK

IJR-4000 SERIES

- IJR-4000 FW100 / FW200
  - Flexible White Legend Ink
- IJR-4000 LW100
  - Rigid White Legend Ink Cured by LED
- IJR-4000 MW300 / MW301
  - Rigid White Legend Ink

IJR-4000 MW300

IJR-4000 FW100

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(30 microns or below), the additive process first removes all the copper from the panel and then adds back the conductive metal to form traces. Consequently, that conductive metal is no longer limited to copper, opening the opportunity to meet this requirement of gold conductors on polyimide. Although the additive process is most often used for fine feature sizes, it can also be applied to larger traces. In this case, the minimum feature size was a 75-micron trace and space.

The challenge with this new process is just that—it is new. There are not decades of experience and quality specifications to rely on, at least not yet. I think designers and fabricators are very good at communicating design requirements via the fab drawing for standard technology. But with something new, in my opinion, the way to be successful is to communicate not only through the fab drawing but with actual conversation. In the recent applications with gold conductors, not only were there discussions before finalizing the design, but there were also conversations throughout the fabrication cycle, bringing all parties together to discuss the progress and results and talk through any recommendations for process and design improvement for future applications.

The challenge with this new process is just that—it is new. There are not decades of experience and quality specifications to rely on, at least not yet.

Complex Rigid-Flex

Another story I would like to share involved a complex rigid-flex design. To some, complex rigid-flex designs are something they are well versed in, but to others, this is a new technology. To provide some context, in this particular application, there was the need for mixed materials, unbalanced copper weights, and no less than 10 different flex areas, with only selective layers going into those different areas.

As is often the case, the team working on this had competing needs that were driving this complexity. Thankfully, understanding that this was quickly becoming a more complicated design than had been done previously, this team reached out to the fabricator for advice and review before jumping in and working on the PCB layout. Again, communication was key to the success of this highly complex design.

There were many conference calls pulling in the full group and the fabricator until the material configuration and layout concept were adjusted to something that was both manufacturable and met the overall design objectives. It would have been a costly mistake to have completed the design and sent it for fabrication without fabricator input. Fabricators are a significant source of knowledge and are happy to share that knowledge early in the design phase.

The Power of Communication

I share these two success stories to illustrate the power of communication, particularly conversations between design and fabrication. During the recent "Just Ask Tara Dunn" series, one of the questions that I was asked was "Why don't flex and rigid fabricators provide more feedback to designers, especially if it's not good design and engineering work?" That is a powerful question that shines a light on the opportunity to improve communication to the benefit of both fabricators and designers.

I cannot imagine a scenario where a designer would not want feedback that would improve the overall design and improve manufacturability. I also cannot imagine a scenario where a fabricator would not be happy to provide that feedback. What I can easily imagine is the impact this improved communication could have on circuit performance, yields, manufacturability, and time to market.

This is an exciting time in the industry. Semi-additive and modified semi-additive PCB processes are being implemented, opening fabrication capabilities that were not previously available, with a significant impact on PCB design. New materials are being released at a rapid pace. The advancements all provide benefits but also come with a learning curve.

My recommendation for successfully navigating that learning curve is to start a dialog with your fabricator as early in the design process as possible. Reach out to learn more about the process or materials that are not familiar. What is the best way to add those requirements to a fabrication drawing? What are the potential challenges to manufacturing with these new processes or materials? How can the design maximize these benefits?

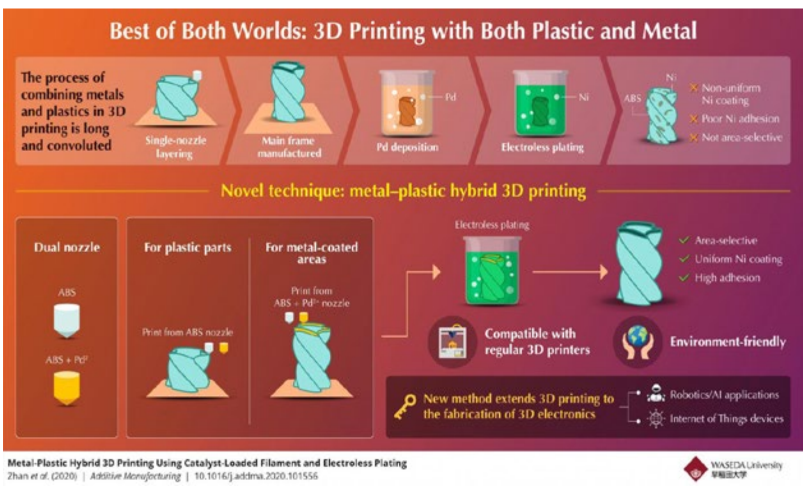
Learning, understanding, and working together will save time, money, and likely plenty of headaches with technology that is new and "outside of the box." **FLEX007**

Tara Dunn is the vice president of marketing and business development for Averatek. To read past columns or contact Dunn, click here.

The Best of Both Worlds: A New Take on Metal-Plastic Hybrid 3D Printing

Scientists from Waseda University, Japan, have developed a metal-plastic hybrid 3D printing technique that produces plastic structures with a highly adhesive metal coating on desired areas.

Also known as "additive manufacturing," 3D printing allows one to create arbitrarily complex 3D objects directly from their raw materials. In fused filament fabrication, the most popular 3D printing process, a plastic or metal is melted and extruded through a small nozzle by a printer head and then immediately solidifies and fuses with the rest of the piece. However, because the melting points of plastics and metals are very different, this technology has been limited to creating objects of either metal or plastic only—until now.



In a recent study published in *Additive Manufacturing,* scientists from Waseda University, Japan, developed a new hybrid technique that can produce 3D objects made of both metal and plastic.

Their method is actually a major improvement over the conventional metallization process used to coat 3D plastic structures with metal. In the conventional approach, the plastic object is 3D-printed and then submerged in a solution containing palladium (Pd), which adheres to the object's surface. Afterwards, the piece is submerged in an electroless plating bath that, using the deposited Pd as a catalyst, causes dissolved metal ions to stick to the object. While technically sound, the conventional approach produces a metallic coating that is non-uniform and adheres poorly to the plastic structure.

In contrast, in the new hybrid method, a printer with a dual nozzle is used; one nozzle extrudes standard melted plastic (acrylonitrile butadiene styrene, or ABS) whereas the other extrudes ABS loaded with PdCl2. By selectively printing layers using one nozzle or the other, specific areas of the 3D object are loaded with Pd. Then, through electroless plating, one finally obtains a plastic structure with a metallic coating over selected areas only.

(Source: Waseda University)

Flex007 Highlights

Flex on the Brain: The Future of Neural Interfaces ▶

The SMTA Additive Electronics TechXchange took place virtually on October 14, with presentations from a wide variety of technologists involved in additive processes. Andy Shaughnessy describes how one of the highlights was a presentation titled "Flexible Electronics for Neural Interfaces" by Dr. Jonathan Viventi, assistant professor of biomedical engineering at Duke University.

New DownStream Software Supports Flex, Rigid-Flex, and Embedded Component Designs ▶

Downstream Technologies released new versions of their industry-leading PCB post-processing solutions CAM350/DFMStream V 14.5 and BluePrint-PCB V6. With these releases, both products will now support the importation and visualization of CAD designs containing flex, rigid-flex, and embedded component data in both 2D and 3D views.

Nano Dimension Prices $50 Million Registered Direct Offering ▶

Nano Dimension Ltd., an additively manufactured electronics provider, announced it entered into definitive agreements with investors for the sale of 16,722,000 of the Company's American Depositary Shares at a price of $3.00 per ADS pursuant to a registered direct offering.

Just Ask Tara Dunn: DFM for Flex and Rigid-Flex ▶

First, we asked you to send in your questions for Happy Holden, Joe Fjelstad, John Mitchell, and others in our "Just Ask" series. Now, it's Omni PCB President Tara Dunn's turn! A regular Flex007 columnist, Tara discusses flexible circuits, rigid-flex, and rigid PCBs, as well as RF/microwave technology, microelectronics, and additive processes. Tara is the co-founder of Geek-a-Palooza and a show manager for the SMTA Additive Electronics TechXchange event. She has over 20 years of experience in the PCB industry. We hope you enjoy "Just Ask Tara."

New DuPont Kapton Polyimide Film Addresses Impact of Faster Voltage Rise on Motor Insulation ▶

DuPont Interconnect Solutions, a unit of DuPont Electronics & Imaging, announced the results of a recent research study that show Kapton® ECRC polyimide film provides an eight-fold improvement over standard polyimide films for insulating the conductors found in high-performance traction motors designed for the e-mobility market.

Notion Systems, PV Nano Cell Partner in Digital Printed Electronics ▶

Notion Systems GmbH, a manufacturer of industrial inkjet systems for functional materials, and PV Nano Cell Ltd., a provider of inkjet-based conductive digital printing solutions and producer of conductive digital inks, announced that a non-exclusive agreement was signed between the companies.

SolarWindow Generates Electricity on Flexible Plastics, Glass ▶

SolarWindow Technologies Inc. announced that for the first time ever, the company successfully produced its electricity-generating flexible glass using roll-to-roll processing, a high-speed method typical to commercial manufacturing of tinted window films, digital displays, printed electronics, and semiconductors.

Buried Capacitance Power Planes

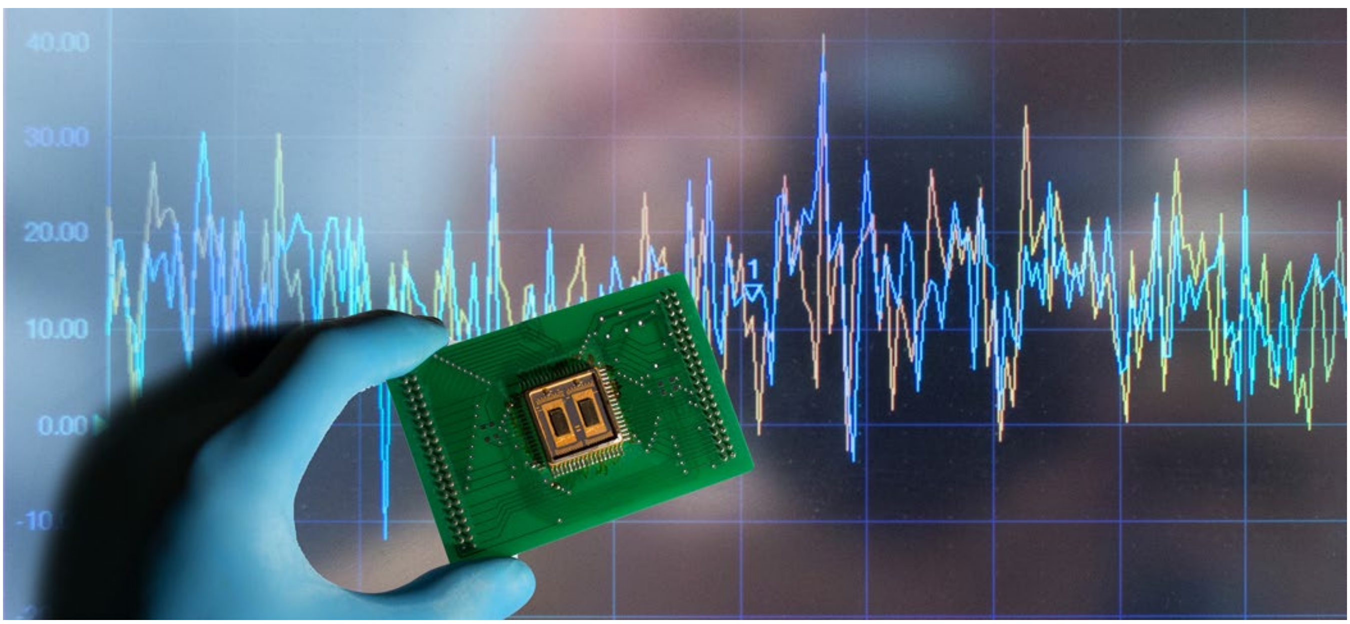
Consider This

by John Talbot, TRAMONTO CIRCUITS

Why do we need capacitance between the power and ground planes? The power planes are just two different levels of voltages. Power is typically at five or three volts, which powers the chips, and ground is zero volts or the return path for the voltage. When you think of voltage, remind yourself it must be a loop. What you send out to power the chip, you have to get back to ground to complete the path. Basic electrical law states that every power or signal line needs a ground or return.

The reason we need capacitance on the power and ground plane is the planes are full of electrical noise, which interferes with the signals. Every time we make the voltage signal turn on or off quickly, such as in a chip or power transistor, we get reflections and noise spikes in the power traces. The quickly rising voltages are driving signals into a low impedance. This causes an initial dip in the power line, then we get a spring-like voltage snap return, which causes a spike, and this electrical noise is embedded right in the power and ground plane signals. To get rid of this electrical noise, we can use the ability of a capacitor to absorb and fill in the electrical voltage variations.

Capacitance acts like a small battery. The capacitor absorbs voltage increases and then releases the stored voltage during a decrease in the present voltage condition. Because the capacitor is like any battery, it can only absorb so much and so fast. The smaller the capacitance value, the faster it can absorb small spikes in voltage (i.e., a small battery is quicker to charge), but the smaller the capaci-



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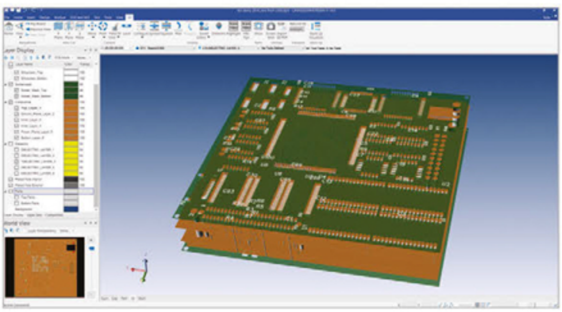

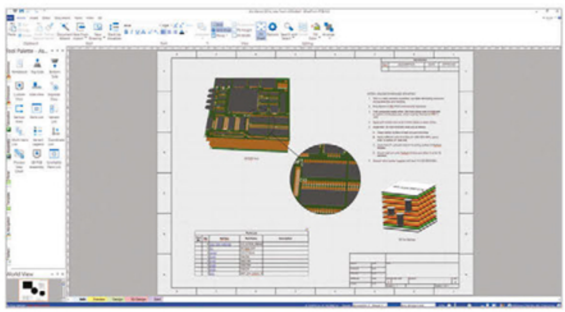

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tance, the less voltage it can accept before it is fully charged. This relates to the frequency of the spike pulses on the power plane.

Small, faster (high-frequency) pulses affecting and creating the noise on the power planes are better absorbed by a small capacitor, such as 200–1000 pF. Larger, lower frequency bumps and spikes from big chips and driver transistors may need larger 0.1–1-nf sized capacitors. Big, very low-frequency pulses, such as power line ripple, are handled by larger capacitors in the 100-mF size.

The capacitor size is its ability to absorb and release energy and is rated in farads. One pF (picofarad) is

10^{-12} farads, nanofarads (nF) is 10^{-9} farads, and a millifarad (mF) is 10^{-6} farads. A small AA-sized battery would be equivalent to a few farads in its ability to absorb and fill in power spikes. As we are trying to reduce the faster noise spikes from switching in the chips, we require the smaller 0.001–0.01-nF sized capacitors.

We have a few choices in embedding capacitance in the power/ground plane, and each has its own good and bad points.

To put the discrete little capacitors at every point needed to absorb chips' pulses would mean mounting hundreds or possibly thousands of small bypass capacitors all over the PCB. These capacitors cost money to put on and QA after assembly, as well as using up valuable PCB real estate. We have a few choices in embedding capacitance in the power/ground plane, and each has its own good and bad points.

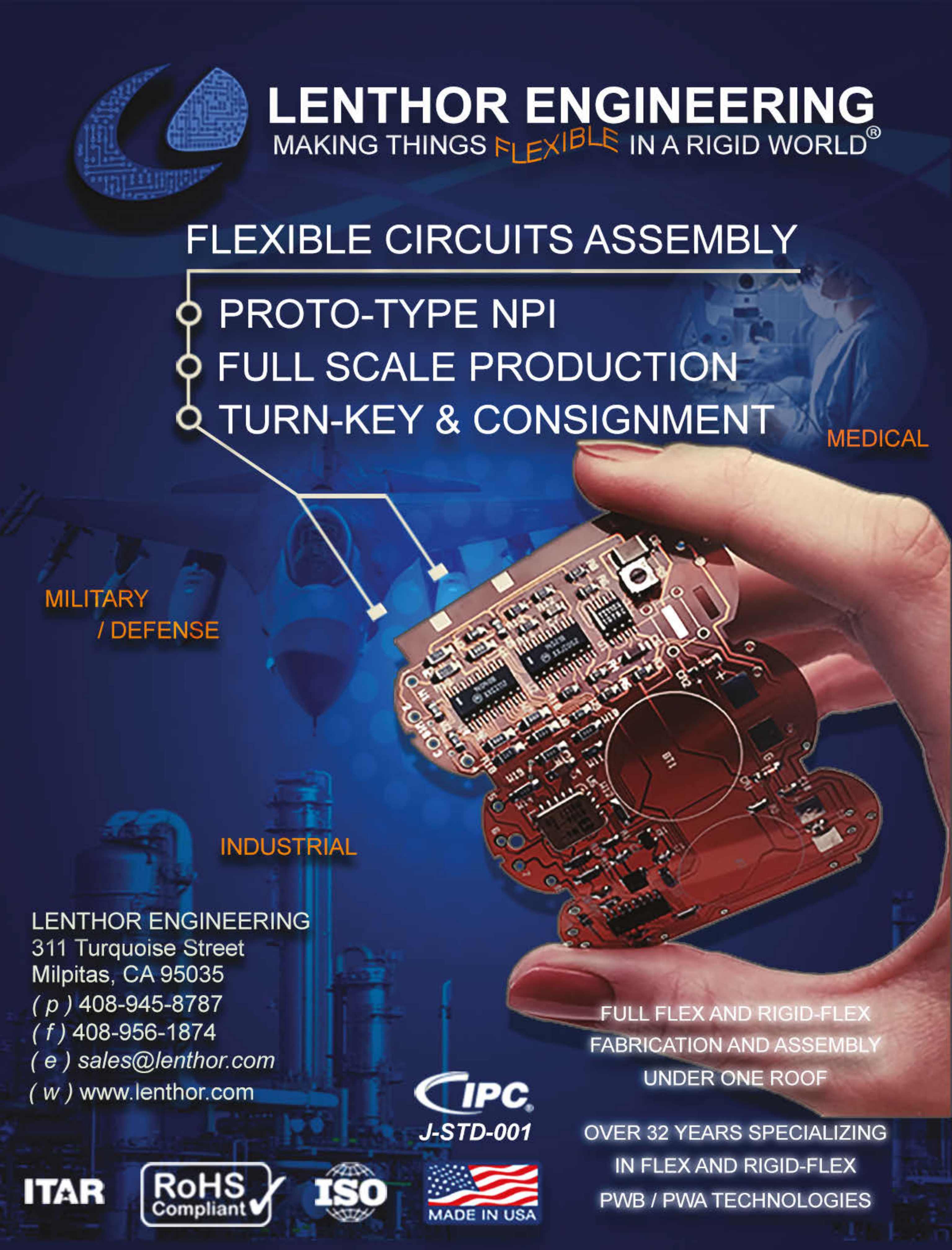
The first is the use of additive films, which have capacitance; they can be imaged and etched. FaradFlex MC25ST, 3M, and DuPont HK04 are some of the most used. A second option is the use of resin-coated copper, such as the RTFoil, or flipped double-treated foil. The thinner laminate layer creates a higher capacitance. The capacitance film applied to the power plane has a very high Dk, which enables higher and better capacitance ratings but still only in the pF range.

Remember that Df is a rating of how well two parallel copper conductors separated by a dielectric retain voltage (i.e., its loss value). Thin 2-mil polyimide films have a further advantage of being lower loss than typical FR-4. The Df of flex PI material is 0.002. The Dk factors of 3.2 and the Df loss factor tells us how fast the stored electrons are leaked off. The high loss Df of FR-4 (0.012) is not great for capacitors, as they leak voltage so quickly as to be more of an absorber than a battery. We call that type of capacitor a snubber.

The most used method to create capacitance between the power and ground plane is to use a very thin layer of FR-4 or flex PI dielectric between the copper layers. The capacitor is made by putting a dielectric (insulator) between two parallel conductors. That is exactly what we have in the normal multilayer ground/power plane core. To make the capacitance large enough to effectively remove the spikes and pulses, we need to increase the capacitance over what is obtained using a typical 5-mil FR-4 or PI core.

To increase capacitance, we have three variables: area, which is predefined by the size of the PCB; increase Dk, which is defined by the laminate used (i.e., FR-4 prepreg at 4.2 Dk, and PI has a Dk of 3.2); or we decrease the distance between the two parallel conductive plates (i.e., thinner laminate between planes).

The easiest to implement is to decrease the spacing between the power and ground copper planes while maintaining reliability and voltage ratings. A 2-mil FR-4 core between two copper conductors has a capacitance of 50–250 pF per square inch. There have been many patents over the years pertaining to different applications of this technology; however, most have expired. Presently, there are quite a few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vendors selling thin 2-mil FR-4 cores with the dendrites facing out to increase voltage rating, where the PI film has a much higher dielectric rating and no need for outward-facing dendrites.

The thin FR-4 cores are dry-filmed, imaged, developed, and then etched as normal, resulting in a power ground plane, which is then laminated into a normal multilayer. The buried capacitance is spread out evenly between the planes. The FR-4 or PI capacitive layer is very effective in suppressing spikes right at the source. The further away the capacitor is from the power pin of the chip, the less effective it is in suppressing the spikes or noise. Buried capacitive FR-4 or PI laminate cores are an easy, low-cost, and effective solution to reduce power plane spikes and noise. **FLEX007**

John Talbot is president of Tramonto Circuits. To read past columns or contact Talbot, click here.

Turning Diamonds Into Metal

Long known as the hardest of all natural materials, diamonds are also exceptional thermal conductors and electrical insulators. Now, researchers have discovered a way to tweak tiny needles of diamond in a controlled way to transform their electronic properties, dialing them from insulating, through semiconducting, all the way to highly conductive, or metallic. This can be induced dynamically and reversed at will, with no degradation of the diamond material.

Their findings are reported this week in the Proceedings of the National Academy of Sciences. The paper is by MIT Professor Ju Li and graduate student Zhe Shi; Principal Research Scientist Ming Dao; Professor Subra Suresh, who is president of Nanyang Technological University in Singapore as well as former dean of engineering and Vannevar Bush Professor Emeritus at MIT; and Evgenii Tsymbalov and Alexander Shapeev at the Skolkovo Institute of Science and Technology in Moscow.

The concept of straining a semiconductor material such as silicon to improve its performance found applications in the microelectronics industry more than two decades ago. In a major advance in 2018, a team led by Suresh, Dao, and Yang Lu from the City University of Hong Kong showed that tiny needles of diamond, just a few hundred nanometers across, could be bent without fracture at room temperature to large strains.

Key to this work is a property known as bandgap, which essentially determines how readily electrons can move through a material. In their latest simulations, the researchers show that diamond's bandgap can be gradually, continuously, and reversibly changed, providing a wide range of electrical properties, from insulator through semiconductor to metal.

This early-stage proof-of-concept work is not yet at the point where they can begin to design practical devices, the researchers say, but with the ongoing research they expect that practical applications could be possible, partly because of promising work being done around the world on the growth of homogeneous diamond materials.

(Source: MIT News Office)


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1 Beyond Design: Routing Strategies for High-Speed PCB Design ▶


Barry Olney

As the typical PCB design becomes more complex, so do the techniques and strategies required. Barry Olney describes why PCB designers need to understand the underlying high-speed issues of the design based on simulation and then translate these into corresponding design constraints.

2 Roundtable Discussion: App Notes and Fab Notes ▶

Dana Korf, Jen Kolar, Mark Thompson, and Kelly Dack, review the June and August 2020 issues of *Design007 Magazine,* which covered app notes and fab notes, respectively. The group discusses some of the ongoing challenges related to incomplete and inaccurate design data and why communication can preclude many of these problems. What follows is the transcript from this conversation.

3 Dana on Data: Reducing PCB Specification Interpretation Issues ▶


Dana Korf

The PCB industry has accepted a low-quality level of provided documentation from its customers for the past several decades. In this column, Dana Korf reviews one common fabrication print note and asks, "How do you interpret this note?"

4 Sensible Design: Top Tips for a Successful Thermal Management Process ▶


Jade Bridges

Jade Bridges concentrates on some of the complications you are likely to encounter when selecting and applying a thermal interface material and looks a little more closely at thermal resistance, viscosity, and vibration, as well as their effects on performance. Read on to learn how to fully optimize your thermal management process.

5 Fresh PCB Concepts: Finding and Qualifying a Long-Term Partner ▶


Ruben Contreras

Finding the right factories is not an easy task. Anyone can take customers' files and send them to whichever factory is available. But what guarantees does the customer have that the factory used is reliable in producing the design? Ruben Contreras details how to find and qualify a long-term partner.

6 The Bare (Board) Truth: Via Basics ▶


Mark Thompson

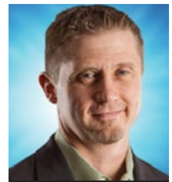
In this month's column, Mark Thompson addresses what vias are and what they are used for, as well as how they are used in PCB design. He also covers some criteria on pad size vs. via size for fabrication and how vias came about.

7 Brad Griffin Discusses Cadence's New Transient Solver Technology ▶


Brad Griffin

Andy Shaughnessy speaks with Brad Griffin, product marketing director for Cadence Design Systems, about their new Clarity 3D Transient Solver, which is designed for system-level EMI simulation. Brad explains how the new solver, based on the company's matrix technology, can yield results 10 times faster than existing solvers when simulating IC packages, PCBs, and SoIC designs.

8 Connect the Dots: The New Recipe for Customer Service Success ▶


Matt Stevenson

How are you holding up these days during the pandemic? Each of us is dealing with life struggles and changes differently. With this in mind, Matt Stevenson asks Al Secchi, global customer support and sales manager, what he has learned professionally from the pandemic and how to serve customers.

9 Time to Market: How Fast Do You Really Need It? ▶


Imran Valiani

There is no doubt that in this fast-paced world of innovation and time to market, speed is one of the most important aspects of making your products and company successful. Imran Valiani shares four actions that can be taken premanufacturing to cut down the critical need for speed at the manufacturing level.

10 Tim's Takeaways: PCB Vias, 'You Have a Go' ▶


Tim Haag

Do you remember the old TV show "Stargate SG-1?" With the exhortation of "SG-1, you have a go" from their commanding officer, the stargate would instantaneously transport an intrepid band of heroes to new and exciting locations each week. Tim Haag details his realization that the stargate is nothing more than a giant via in space!

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Flex007.com focuses on the rapidly growing flexible and rigid-flex circuit market.

Career Opportunities

Now Hiring

Director of Process Engineering

A successful and growing printed circuit board manufacturer in Orange County, CA, has an opening for a director of process engineering.

Job Summary:

The director of process engineering leads all engineering activities to produce quality products and meet cost objectives. Responsible for the overall management, direction, and coordination of the engineering processes within the plant.

Duties and Responsibilities:

- Ensures that process engineering meets the business needs of the company as they relate to capabilities, processes, technologies, and capacity.
- Stays current with related manufacturing trends. Develops and enforces a culture of strong engineering discipline, including robust process definition, testing prior to production implementation, change management processes, clear manufacturing instructions, statistical process monitoring and control, proactive error proofing, etc.
- Provides guidance to process engineers in the development of process control plans and the application of advanced quality tools.
- Ensures metrics are in place to monitor performance against the goals and takes appropriate corrective actions as required. Ensures that structured problem-solving techniques are used and that adequate validation is performed for any issues being address or changes being made. Develops and validates new processes prior to incorporating them into the manufacturing operations.
- Strong communication skills to establish priorities, work schedules, allocate resources, complete required information to customers, support quality system, enforce company policies and procedures, and utilize resources to provide the greatest efficiency to meet production objectives.

Education and Experience:

- Master's degree in chemical engineering or engineering is preferred.
- 10+ years process engineering experience in an electronics manufacturing environment, including 5 years in the PCB or similar manufacturing environment.
- 7+ years of process engineering management experience, including 5 years of experience with direct responsibility for meeting production throughput and quality goals.

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Now Hiring

Process Engineering Manager

A successful and growing printed circuit board manufacturer in Orange County, CA, has an opening for a process engineering manager.

Job Summary:

The process engineering manager coordinates all engineering activities to produce quality products and meet cost objectives. Responsible for the overall management, direction, and coordination of the engineering team and leading this team to meet product requirements in support of the production plan.

Duties and Responsibilities:

- Ensures that process engineering meets the business needs of the company as they relate to capabilities, processes, technologies, and capacity.
- Stays current with related manufacturing trends. Develops and enforces a culture of strong engineering discipline, including robust process definition, testing prior to production implementation, change management processes, clear manufacturing instructions, statistical process monitoring and control, proactive error proofing, etc.
- Ensures metrics are in place to monitor performance against the goals and takes appropriate corrective actions as required. Ensures that structured problem-solving techniques are used and that adequate validation is performed for any issues being address or changes being made. Develops and validates new processes prior to incorporating into the manufacturing operations

Education and Experience:

- Bachelor's degree in chemical engineering or engineering is preferred.
- 7+ years process engineering experience in an electronics manufacturing environment, including 3 years in the PCB or similar manufacturing environment.
- 5+ years of process engineering management experience, including 3 years of experience with direct responsibility for meeting production throughput and quality goals.

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IPC instructors will conduct training at one of our public training centers or will travel directly to the customer's facility. A candidate's close proximity to Longmont, CO, or Phoenix, AZ, is a plus. Several IPC Certification Courses can be taught remotely and require no travel.

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Candidates must have a minimum of five years of electronics manufacturing experience. This experience can include printed circuit board fabrication, circuit board assembly, and/or wire and cable harness assembly. Soldering experience of through-hole and/or surface-mount components is highly preferred.

Candidate must have IPC training experience, either currently or in the past. A current and valid certified IPC trainer certificate holder is highly preferred.

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- Identify preliminary market strategies to develop specific offerings
- Provide training on application technologies and specific products to sales and technical personnel
- Support new product development by determining customer needs and communicating these needs to the proper technical group(s)/product managers
- Network with relevant industry players to obtain market information/facilitate partnerships
- Perform other duties or special projects as assigned

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Our Summit Anaheim, CA, division currently has multiple open positions for planning engineers.

The planner is responsible for creating and verifying manufacturing documentation, including work instructions and shop floor travelers. Review lay-ups, details, and designs according to engineering and customer specifications through the use of computer and applications software. May specify required manufacturing machinery and test equipment based on manufacturing and/or customer requirements. Guides manufacturing process development for all products.

Responsibilities:

1. Accurately plan jobs and create shop floor travelers.
2. Create documentation packages.
3. Use company software for planning and issuing jobs.
4. Contact customers to resolve open issues.
5. Create TDR calculations.
6. Assist in the training of new planning engineers.
7. Review prints and purchase orders.
8. Create stackups and order materials per print/spec.
9. Plan jobs manufacturing process.
10. Institute new manufacturing processes and or changes.

Education/Experience:

1. High school diploma or equivalent
2. Minimum five (5) years' experience in the printed circuit board industry with three (3) years as a planning engineer.
3. Must be able to cooperate and communicate effectively with customers, management, and supervisory staff.
4. Must be proficient in rigid, flex, rigid/flex, and sequential lam designs.

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Career Opportunities

SMT Operator
Hatboro, PA

Manncorp, a leader in the electronics assembly industry, is looking for a **surface-mount technology (SMT) operator** to join their growing team in Hatboro, PA!

The **SMT operator** will be part of a collaborative team and operate the latest Manncorp equipment in our brand-new demonstration center.

Duties and Responsibilities:

- Set up and operate automated SMT assembly equipment
- Prepare component kits for manufacturing
- Perform visual inspection of SMT assembly
- Participate in directing the expansion and further development of our SMT capabilities
- Some mechanical assembly of lighting fixtures
- Assist Manncorp sales with customer demos

Requirements and Qualifications:

- Prior experience with SMT equipment or equivalent technical degree preferred; will consider recent graduates or those new to the industry
- Windows computer knowledge required
- Strong mechanical and electrical troubleshooting skills
- Experience programming machinery or demonstrated willingness to learn
- Positive self-starter attitude with a good work ethic
- Ability to work with minimal supervision
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We Offer:

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- Retirement fund matching
- Continued training as the industry develops

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SMT Field Technician
Hatboro, PA

Manncorp, a leader in the electronics assembly industry, is looking for an additional SMT Field Technician to join our existing East Coast team and install and support our wide array of SMT equipment.

Duties and Responsibilities:

- Manage on-site equipment installation and customer training
- Provide post-installation service and support, including troubleshooting and diagnosing technical problems by phone, email, or on-site visit
- Assist with demonstrations of equipment to potential customers
- Build and maintain positive relationships with customers
- Participate in the ongoing development and improvement of both our machines and the customer experience we offer

Requirements and Qualifications:

- Prior experience with SMT equipment, or equivalent technical degree
- Proven strong mechanical and electrical troubleshooting skills
- Proficiency in reading and verifying electrical, pneumatic, and mechanical schematics/drawings
- Travel and overnight stays
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We Offer:

- Health and dental insurance
- Retirement fund matching
- Continuing training as the industry develops

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APCT, a leading manufacturer of printed circuit boards, has experienced rapid growth over the past year and has multiple opportunities for highly skilled individuals looking to join a progressive and growing company. APCT is always eager to speak with professionals who understand the value of hard work, quality craftsmanship, and being part of a culture that not only serves the customer but one another.

APCT currently has opportunities in Santa Clara, CA; Orange County, CA; Anaheim, CA; Wallingford, CT; and Austin, TX. Positions available range from manufacturing to quality control, sales, and finance.

We invite you to read about APCT at APCT.com and encourage you to understand our core values of passion, commitment, and trust. If you can embrace these principles and what they entail, then you may be a great match to join our team! Peruse the opportunities by clicking the link below.

Thank you, and we look forward to hearing from you soon.

apply now

Career Opportunities

U.S. CIRCUIT

Sales Representatives (Specific Territories)

Escondido-based printed circuit fabricator U.S. Circuit is looking to hire sales representatives in the following territories:

- Florida
- Denver
- Washington
- Los Angeles

Experience:

- Candidates must have previous PCB sales experience.

Compensation:

- 7% commission

Contact Mike Fariba for more information.

mfariba@uscircuit.com

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